Wideband harmonic control of high efficiency high power GaN amplifiers in S-Band and power packaging issues.

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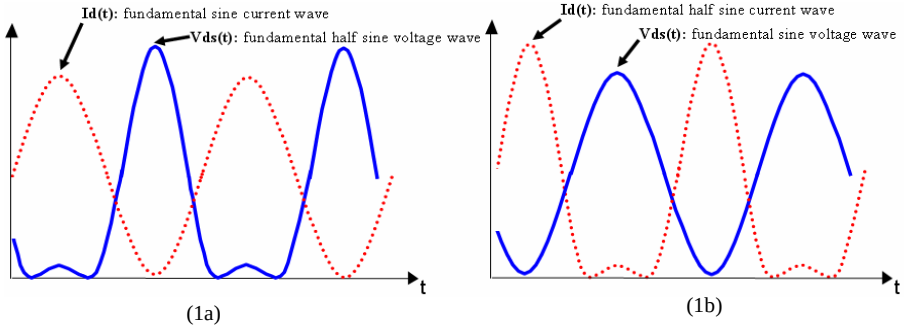
INTRODUCTION

Radar applications require more and more trade off between power added efficiency (PAE) and output power over wider frequency bandwidths. To obtain such results, the dissipated power has to be reduced as low as possible. Thus, enhancement of PAE will decrease constraints on thermal management, dimensioning and reliability. GaN HEMTs offer a great potential in terms of power added efficiency, output power density and capability to handle high temperature.
Peak PAE performances close to 80% have been published [1]-[2] for class-F and inverse class-F GaN power amplifiers operating in S-Band. Nevertheless, the limited bandwidths of these amplifiers are not suitable for radar applications. Over 10% bandwidth in S-Band, an inverse class-F amplifier [3] exhibits more than 60% drain efficiency and 10W output power. At 3.5GHz, a peak PAE of 78% is associated to 12dB gain and 11W output power. Moreover, when using 2nd-harmonic input tuning, a class-E GaN power amplifier [4] exhibits peak PAE of 74% and 12W output power from 2.0 to 2.5GHz. The best broadband performances are obtained from 2.1 to 2.7GHz without 2nd-harmonic input tuning where PAE is between 53% and 66%. An experimental work on GaN HEMT at 2GHz [5] shows that PAE could be improved by 25 points when the transistor operates in class-F with 2nd-harmonic input tuning. This work reports a methodology to control the 2nd harmonic output load of GaN HEMTs over 20% bandwidth in S-Band for radar applications.
The first section presents the impact of 2nd harmonic output impedances on time domain voltage and current waveforms. The second section describes on-wafer load-pull measurements performed on a 6x400µm GaN HEMT from UMS. The third section is dedicated to simulated and measured results of the synthesized loads at fundamental and 2nd harmonic over a large bandwidth in S-Band. The power measurements are performed within the package reference plane in order to highlight the great impact of controlling the 2nd harmonic output load in terms of PAE, and to demonstrate the capability of reaching higher bandwidths. The last section reports the issue of package modeling. Package simulations exhibit the impact of lead-frame characteristic impedance in term of PAE for the GaN HEMT.

TIME-DOMAIN ANALYSIS OF THE INFLUENCE OF SECOND HARMONIC LOAD



(1a) (1b)

Fig. 1 Output voltage and current waveforms when an open circuit (a) or a short circuit (b) are presented at the 2nd harmonic frequency.

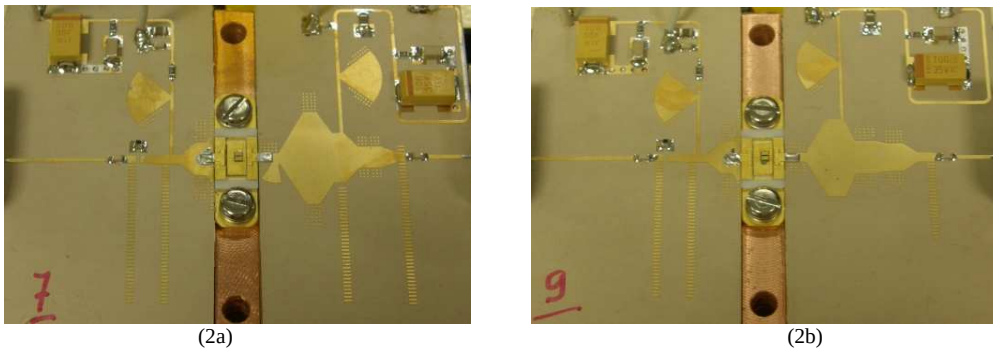
Switching operating classes are obtained when load impedances are controlled for all harmonics. In practice, the loads at the first three harmonic frequencies are controlled.
According to the operating class, voltage and current output waveforms are a combination of quasi square wave and half sine wave. The overlapping between both waves is minimized so that to provide the efficiency enhancement.
In this reported work, only the 2nd-harmonic output tuning is handled to optimize the PAE over a larger bandwidth. Figure 1 presents two waveform cases when only the 2nd harmonic load is adjusted. In case (a), an open circuit is presented at the 2nd harmonic frequency to generate a half sine voltage wave. In case (b), a half sine current wave is obtained by synthesizing a short circuit at the 2nd harmonic frequency.

ON-WAFER LOAD-PULL MEASUREMENTS

On-wafer Load-Pull measurements [6] have been performed on a 2.4mm (6x400µm) HEMT GaN from UMS. The applied RF power is pulsed using 10µs width and 10% duty cycle. Biasing voltages are also pulsed to 50V drain voltage. The output loads at fundamental and 2nd harmonic frequencies are tuned to reach the maximum PAE.
At f_0 which is the center frequency of the bandwidth, the transistor exhibits 42.5dBm output power associated to 61% PAE and 12.5dB power gain at 2.5dB compression when only the output load is optimized at the fundamental frequency. When the output load is tuned at the 2nd harmonic to reach a maximum PAE, the device performances are improved to reach 65% PAE at the same input power while power gain and output power remain identical. The PAE enhancement would have been better if the multi-harmonic tuner had been able to present impedances at boundaries of the Smith chart. The same measurement process has been applied at f_{min} and f_{max} to reach the optimum PAE.
While the interest of controlling the 2nd harmonic output load is demonstrated for this power device, the capability of synthesizing the required output loads at harmonics over the whole bandwidth is now reported.

DESIGN AND REALISATIONS OF MATCHING CIRCUITS AND MEASUREMENTS RESULTS.

At first, the GaN chip has been packaged. One bond wire is brazed on the gate and two parallel bond wires were soldered on the drain. Four source pads were connected to the ground using one bond wire. All bond wires have 38µm diameter. The different elements of the power package were considered in simulations.
Starting from on-chip load-pull measurements of the device and considering the package influence, two power amplifiers were designed to investigate the capabilities of bandwidth enhancement at maximum PAE for radar applications. The first power amplifier has been designed to control only the fundamental output load while the other one has been optimized at fundamental and 2nd harmonic all over the required 20% bandwidth. Figure 2 shows photographs of the two power amplifiers with and without the 2nd harmonic control. The input matching circuit is the same for the two amplifiers and was designed to obtain an input matching S11<-10dB over the bandwidth. Input and output matching circuits were simulated with ADS momentum software. Matching circuits were implemented on a Rogers duroïd 6010.2LM (ε_r=10.2, H=635µm).

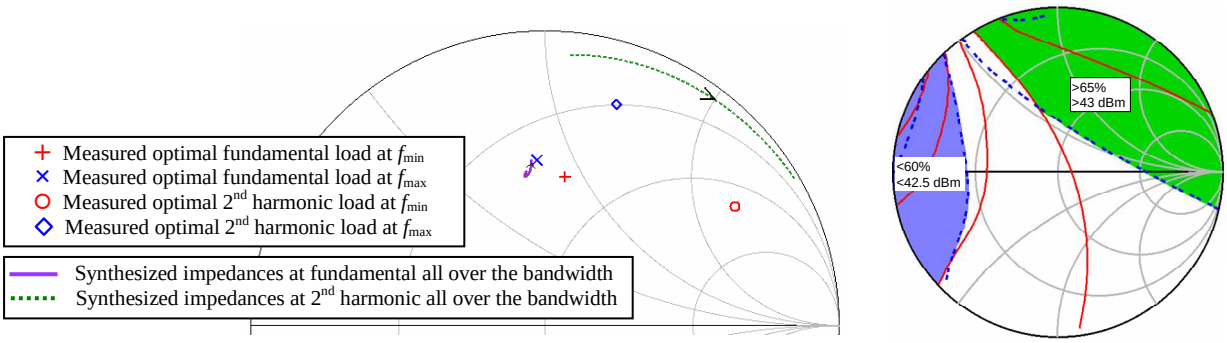


(2a) (2b)

Fig. 2. Power amplifiers with optimized 2nd harmonic (a) and without optimized 2nd harmonic (b).

Within the output matching circuit of power amplifiers, a specific profile of tapered lines is used to enhance the bandwidth performance of load transformation while the 2nd harmonic is controlled using a radial stub placed at around λ/4 from the output of the packaged device (Fig 2.a). The fundamental load is tuned over the bandwidth to reach the best trade off between constant PAE circles higher than 60% at f_{min} and f_{max}. Figure 3.a shows how the simulated

synthesized impedances (output matching circuit) track the loci of the optimum required impedances previously determined by load-pull measurements. This 2nd harmonic impedance matching ensures the chip to be loaded optimally so that the PAE is higher than 65% and exhibit an output power higher than 43 dBm as shown in figure3.b. Load pull simulations at the second output harmonic ($2xf_{min}$) of the nonlinear electro-thermal model allow us to discern the optimal and worst areas in terms of output power and PAE.



(3a) (3b)

Fig. 3. Comparison of targeted synthesized and measured output loads at fundamental and 2nd harmonic over the frequency bandwidth (3.a). Simulated constant PAE and Pout circles at 2nd harmonic output ($2xf_{min}$) (3.b).

The two power amplifiers have been characterized at Thalès Air Systems. Transistor power amplifiers are biased near the pinch off voltage and drain bias voltage is set to 50V. Biasing voltages are continuous while the input RF signal is pulsed (10µs/10%). A TRL calibration process has been used to determine the power performances within the package reference plane in order to compare the two measures of power amplifiers with and without 2nd harmonic output tuning. The measurement results in terms of output power, gain and PAE are presented in table I at f_{min}, f_0 and f_{max} for the two versions of the power amplifier.

Table 1. Measurements results within package reference plans of both amplifiers

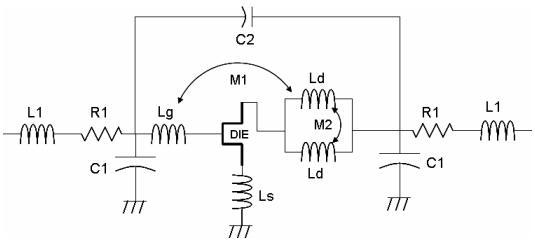
	Measured Results with Optimized Second Harmonic Load			**Measurement Results without Optimized Second Harmonic Load**		
Frequencies	f_{min}	f_0	f_{max}	f_{min}	f_0	f_{max}
Pin (dBm)	28.5	28.3	28.5	28.6	28.4	28.3
Pout (dBm)	43.7	43.1	43.1	42.8	42.6	41.9
Gain (dB)	15.2	14.8	14.6	14.2	14.2	13.6
PAE %	69	63	67	57	55	52

The best performances in terms of output power, gain and PAE are obtained in the case of the power amplifier for which the 2nd harmonic output load was optimized. At f_{min}, f_0 and f_{max}, the power added efficiency shows an increase of 12, 8 and 15 points while the output power enhancement is between 0.5dB and 1.2dB. For all presented results, compression gain is between 2dB and 2.5dB. Over the 20% bandwidth, the optimised power amplifier demonstrates more than 63% PAE, 20W output power (>8.5W/mm) and 14.6 dB gain. The peak power added efficiency (69%) is obtained at f_{min} with 43.7dBm output power (9.7W/mm) and 15.2dB power gain.
Besides performances, the comparison between the two power amplifiers allows us to quantify the impact of optimised 2nd harmonic controlled on 20% bandwidth in S-Band.

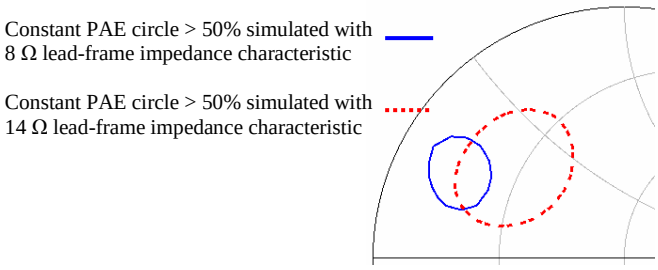
PACKAGING ISSUES

A Test fixture with input and output lines has been realized to receive the package. An electrical package model [7] has been extracted from on-wafer and test fixture S-parameter measurements. S-parameters within package reference planes were calculated by de-embedding the input and output lines of test fixture. The electrical model (figure 4.a) has been fitted and compared to de-embedded S-parameters. Gate, drain and ground bond wires are respectively modeled by equivalent inductors Lg, Ld and Ls. Mutual inductances are accounted for the inductive coupling between both drain

wires (M2) and between gate and drain wires (M1). Capacitances (C1) represent input and output lead-frames, which are connected by a coupling capacitance (C2). Constant PAE circles have been simulated within reference package plane at f_{min} for two characteristic impedances of lead-frame (figure 4.b). In this package, the characteristic impedance is around 8 Ω. If the line width of lead-frame decreases, the equivalent capacitance (C1) is lower. Two packaged transistor simulations were performed for 8 Ω and 14 Ω lead-frame characteristic impedances. Thus, for a smaller width of lead-frame, constant PAE circle is wider so that impedance matching at fundamental becomes easier.



(4a)



(4b)

Fig. 4. Equivalent circuit of ceramic package (4.a). Constant PAE circles comparison within reference package plane for two lead-frame impedance characteristics at f_{min} (4.b).

CONCLUSIONS

This paper reports the comparison of two design methodologies with and without controlling the 2nd harmonic output loads in 20% bandwidth in the case of high power packaged GaN HEMT. Besides performances, the power measurements of both power amplifiers allow us to quantify the impact of optimized 2nd harmonic on power added efficiency and the capability of reaching wider operating bandwidths. These results are strong promising and open many directions of improvements such as matching architectures, operating bandwidth and device size.
The package used for power amplifier design is of prime importance. Studies will be realized to determine the most appropriate package contingent on chip characteristics.

ACKNOWLEDGMENT

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REFERENCES

[1] David Schmelzer and Stephen I. Long “A GaN HEMT Class F Amplifier at 2 GHz with >80% PAE” Compound Semiconductor Integrated Circuit Symposium, pp. 96-99, Nov. 2006.
[2] P. Wright, A. Sheikh, C. Roff, P.J. Tasker and J. Benedikt. “Highly Efficient Operation Modes in GaN Power Transistors delivering Upwards of 81% Efficiency and 12W Output Power” IEEE MTT-S, pp 1147-1150, June 2008.
[3] P. Saad, H.M. Nemati, M. Thorsell, K. Andersson and C. Fager “An Inverse Class-F GaN HEMT Power Amplifier with 78% PAE at 3.5 GHz”, European Microwave Conference, pp 496-499, Oct. 2009.
[4] Mark P. van der Heijden, Mustafa Acar, and Jan S. Vromans. “A Compact 12-Watt High-Efficiency 2.1-2.7GHz Class-E GaN HEMT Power Amplifier for Base Stations” IEEE MTT-S, pp 657-660, June 2009.
[5] A. Ramadan, A. Martin, T. Reveyrand, J.M. Nebus, P. Bouysse, L. Lapierre, J.F Villemazet, S. Forestier. “Efficiency enhancement of GaN power HEMTs by controlling gate-source voltage waveform shape” European Microwave Conference, pp 1840-1843, Oct. 2009.
[6] D. Barataud, M. Campovecchio, J-M. Nebus. “Optimum design of very high-efficiency microwave power amplifiers based on time-domain harmonic load-pull measurements” IEEE Transactions on Microwave Theory and Techniques, vol. 49, issue 6, pp. 1107-1112.
[7] Tao Liang, Member, IEEE, Jaime A. Plá, Member, IEEE, Peter H. Aaen, Member, IEEE, and Mali Mahalingam. “Optimum Equivalent-Circuit Modeling and Verification of Metal–Ceramic Packages for RF and Microwave Power Transistors” IEEE Transactions on Microwave Theory and Techniques, vol. 47, NO. 6, JUNE 1999.