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Power and thermal design criteria of AlGaN/GaN cascode cell for wideband distributed power amplifier

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***Abstract*—This paper deals with non-linear modeling of power GaN HEMT and design of power balanced cascode cell for wideband distributed power amplifiers. The active device is a 8x50µm AlGaN/GaN HEMT grown on SiC substrate. The cascode die is flip-chipped onto an AlN substrate via electrical and mechanical bumps. This GaN-based cascode cell is dedicated to act as the unit power device within a broad-band capacitively-coupled 4-18GHz distributed amplifier.**

Keywords-component; AlGaN/GaN HEMT modelling, balanced cascode cell, flip-chip, gallium nitride.

I. INTRODUCTION

The emergent GaN HEMTs (High Electron Mobility Transistor) devices are promising for power amplification due to their excellent material properties: they have high breakdown voltage with high cutoff frequency compared to the other material based devices, leading to high power and high efficiency amplifiers for next generation wireless communication, satellite communication and radar systems. Famous abilities have been demonstrated by several papers [1], [2]. The capability of generating high RF output power makes AlGaN/GaN HEMTs an appealing alternative to traditional GaAs and InP devices.

This paper deals with the non-linear modeling of GaN HEMTs device and the power optimization of cascode cells to be integrated in 4-18GHz distributed amplifiers. Thermal issues of the cascode cell is analyzed and controlled to prevent each device from thermal failure. An aluminum nitride flip-chip substrate (AlN) presenting a high thermal conductivity ($170W.m^{-1}.K^{-1}$) is used to have a good thermal dissipation [3].

II. LINEAR & NON- LINEAR MODELLING

The device considered in this paper is a 400µm coplanar AlGaN/GaN HEMT (8x50µm) of 1.5µm-gate length processed on a silicon carbide substrate form Tiger Laboratory.

A. Linear model

The first analysis to be led concerns the extraction of the small signal model of the transistor. All parameters have been extracted from pulsed scattering [S] parameters measurements in the (2-40)GHz frequency band which are measured for each point of the I(V) networks.

This model includes two different parts:

- Extrinsic elements linked up to the die accesses (8 parameters).
- Intrinsic elements corresponded to the active device (7 parameters).

Fig.1 details the small signal model topology.

A dedicated extraction method is used to find all model components: the linear model is calculated with an optimization loop (simulated annealing method) with a cost function meaning that the calculated intrinsic parameters are frequency independents. Extrinsic parameters have to be constant at any bias point while the intrinsic parameters are bias dependent.

The linear model is defined at a specific bias point selected for the future amplifier application.

Fig.2 presents the comparison between model and measurements over the 2-40GHz frequency band and demonstrates the good agreement obtained.

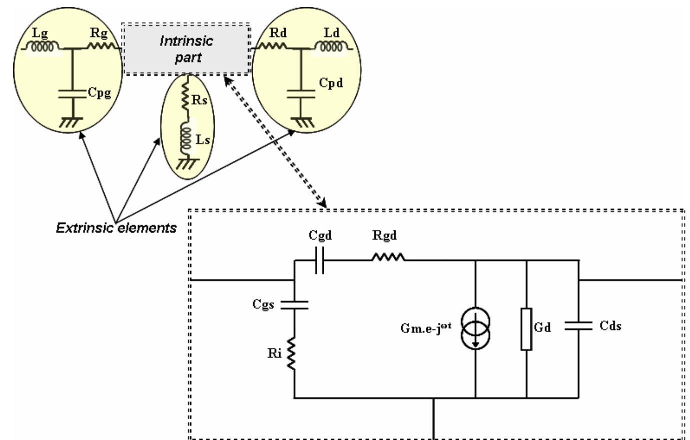

Figure 1. Small signal model topology.

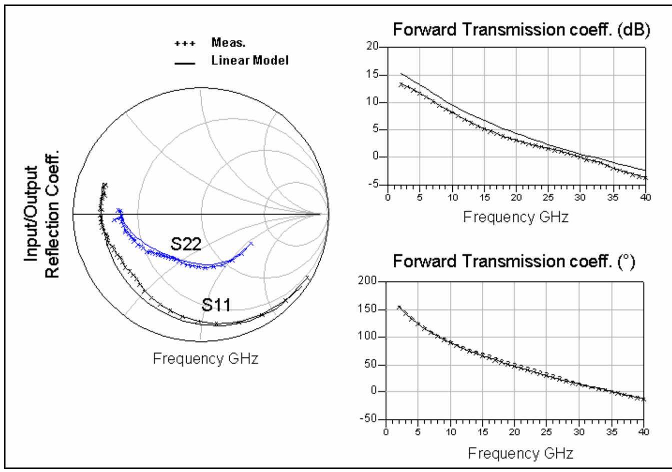

Figure 2. Comparison between simulated and measured scattering parameters at (Vgs_0=-7V, Vds_0=22.6V) quiescent bias point.

B. Non linear model

So as to obtain the non linear model with the current source parameters and then the static characteristics [4], pulsed I-V measurements are performed at room temperature up to 45V of Vds (Fig.3). A drain current density of 1.45A/mm is obtained at the quiescent bias point (Vgs_0=-7V, Vds_0=22.6V). The current source is modeled by Tajima's equation included up to 14 parameters.

Thanks to dedicated software developed at XLIM laboratory, the non linear model parameters are directly extracted knowing the extrinsic resistors form [S] parameters characterization.

The parameters of the breakdown generator and the input diodes are extracted from this measurement. The breakdown is directly described by exponential increases of the gate and drain currents when the breakdown voltage is reached while the diodes are modeled as non linear current sources with Shockley equation.

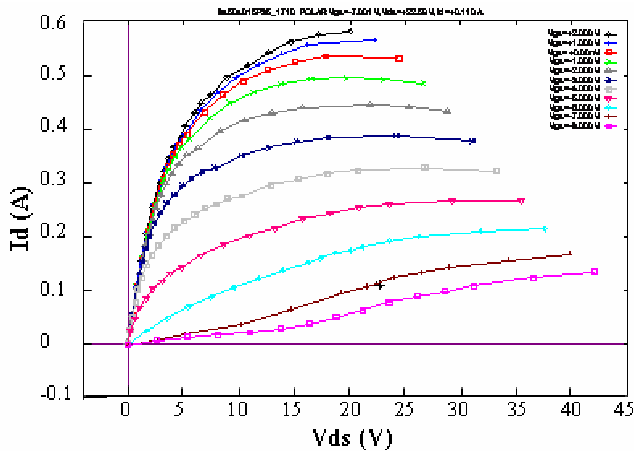

Figure 3. Pulsed I-V characteristic of 8x50µm device measured at quiescent bias point (Vgs_0=-7V, Vds_0=22.6V).

$$Ibk = Ibk_{DG}.\exp_soft(\alpha_{DG}.V_{DS})$$

$$\text{with } \exp_soft = if\,(x < \max_arg)\, then \exp(x), \; else \max_\exp.(x + 1 - \max_arg)$$

$$\max_arg = \ln(\max_\exp); \max_\exp = 10^{99}$$

$$Id_{GD} = Isgd.(e^{\alpha - GD.Vgd} - 1)$$

$$Id_{GS} = Isgs.(e^{\alpha - GS.Vgs} - 1)$$

Cgs and Cgd non linear capacitances are describes by hyperbolic tangent equations as a function of its own control voltage (Vgs and Vgd). These values are extracted along a specific load line on the I-V networks for AB class operation by multibias S parameters extraction.

This model has been implemented in a commercial simulation environment in order to design the optimum power cascode cell.

III. BALANCED CASCODE CELL FOR BROADBAND AMPLIFIER

The cascode cell considered in this part is dedicated to the design and optimization of a 4-18GHz flip-chip distributed power amplifier [5].

The design procedure makes necessary to optimize the power performance of the cascode cell on the bandwidth. Thus, an additional series capacitor Ca_1 is placed on the gate of the second transistor to fix the power matching between transistors independently of frequency. The schematic is represented on Fig.4.

For an optimal transfer between transistor T1 to transistor T2 the drain pad of the first transistor is connected to the source metallization which is distributed on both sides of the transistor T2.

An additional resistance Rstab of 15Ω has been added in series with Ca_1 but integrated onto the AlN substrate to stabilize the cascode cells by avoiding any potential oscillations. As a supplement to the Rollet criterion, the Fig.5 presents the simulated normalized determinant function (NDF) checking the intrinsic stability of the active cascode cell.

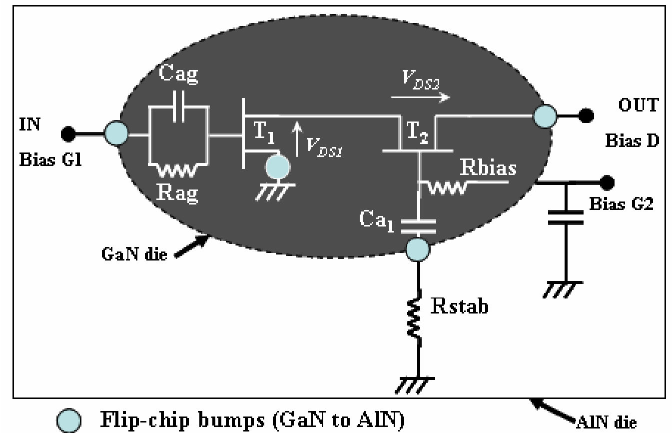

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Figure 4. Schematic of the power cascode cell (GaN die flip-chipped onto AlN).

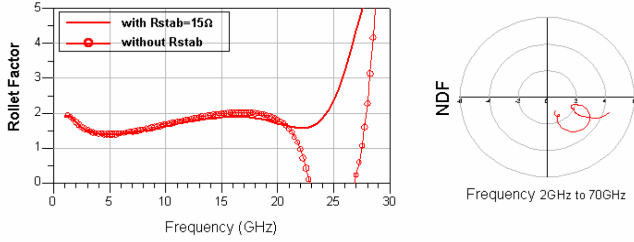

Figure 5. Influence of Rstab on Rollet factor and NDF of the cascode cell.

To establish the open loop analysis, the electrical device models have been transformed [6]. The stability of the cascode cell is one of essential criteria during the design for power optimization. Fig.5 demonstrates the effect and the importance of Rstab for the stabilization at high frequency (e.g. 25GHz).

Besides, the cascode cell has to be optimized for wideband power operation within distributed amplifier. Given the required maximum frequency of 18GHz, it is primordial to adopt a capacitively coupled distributed architecture [7] in order to meet the condition of 50Ω input matching and maximum cut-off frequency of the artificial input gate line. Therefore, the capacitive coupling has been integrated on the GaN cascode cell by adding a series capacitance Cag of 0.3pF on the gate G1 of T1 to reach an acceptable equivalent capacitance of the distributed gate line Cgs_{eq}. The series capacitors Cag dedicated to coupling the cascode cell to the artificial gate line of a distributed amplifier are shunted by implanted resistors Rag of 500Ω in order to supply the gate bias path since there is no DC current flowing through the transistors (Fig.4).

To separately test the balanced cascode cell, a specific AlN die has been designed (Fig.6). The flip-chip AlN circuit also integrates all the via-holes that permit to ground transistors and matching elements. The AlN die integrates the stability resistance Rstab and the gate bias pads of the transistor T2 (V_{BIAS_G2}). V_{BIAS_G1} and V_{BIAS_D} are supplied by the on-wafer probes.

The design of the cascode cell has been performed with the help of the ADS software.

In order to ensure reliable results, hybrid simulations have been performed using electrical and electromagnetic analyses taking into account the specific layout of interconnections between the 2 devices of the cascode cell. The structure has been first optimized through non-linear circuit simulations while the resulting layout has been electromagnetically analyzed to check for any parasitic coupling effect and correct it.

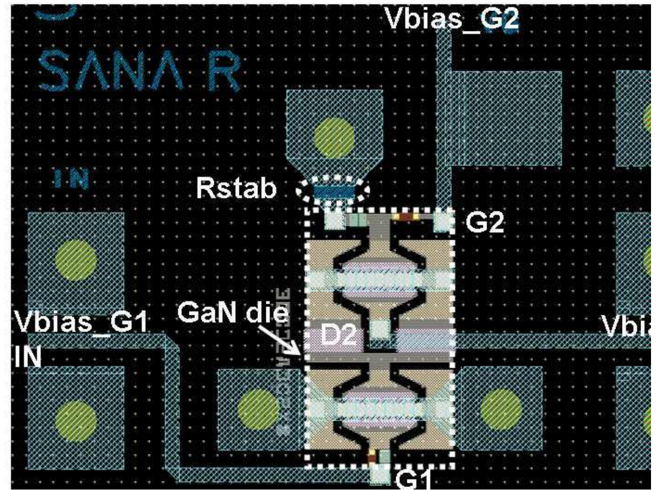

Figure 6. Layout of the AlN die design with flip-whipped GaN cascode cell.

The thermal resistance of this 8x50µm device in standard report is around 35°C/W. Thermal simulations showed that this value is increased by a factor of 1.33 in flip-chip configuration what gives the 47°C/W value. Considering a maximum junction temperature of 35°C, the maximum dissipated power should not exceed 3.5W. Fig.7 shows the simulated dissipated power of each active device of the cascode cell at 20dBm input power.

One can note a maximum value of dissipated power of 3.4W reached by the 2nd transistor at 5GHz. So the cascode cell should be measured imperatively under RF and DC pulsed conditions to avoid any thermal induced failure of the active devices because it is extremely close to the limit of 3.5W.

IV. Measurements

A. *Scattering parameters measurements*

In order to check the accuracy of the linear and nonlinear modeling of the balanced cascode cell, on-wafer S-parameters measurements have been performed in the 0.5-20GHz bandwidth as shown on Fig.8.

The comparison of simulated and measured S-parameters demonstrates a good agreement. It is interesting to note that the gain of the balanced cascode cell is quite flat in the beginning of bandwidth while it is not true for a single transistor.

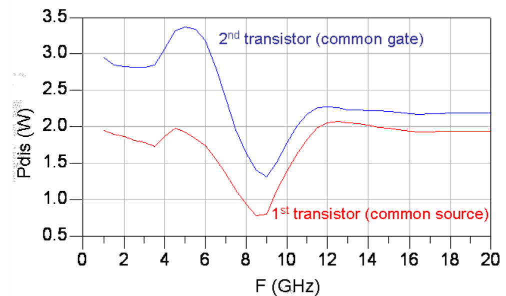

Figure 7. Simulated dissipated power of active devices versus frequency for 20dBm input power.

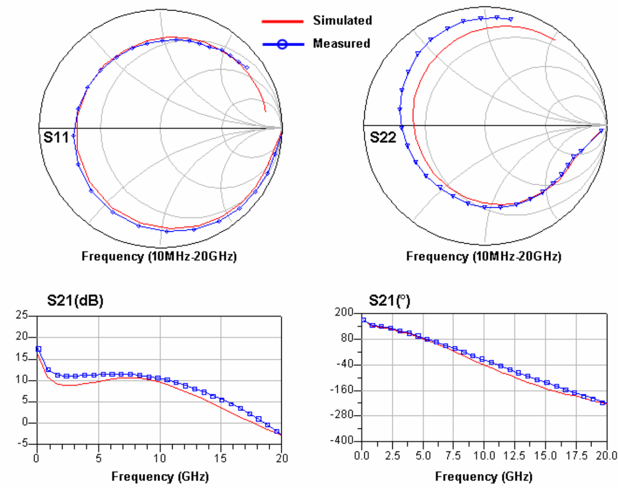

Figure 8. Comparison of simulated and measured S-parameters of the cascode cell.

B. Pulsed load-pull measurement

On-wafer pulsed Load-Pull measurements of the cascode cell have been performed in order to check and compare the optimum power state optimized from nonlinear simulations with power measurements. During the power Load-Pull characterization, the pulses were 10µs width according to a 10% duty cycle. Both RF signals and biases were pulsed.

Fig.9 illustrates the great power performance obtained (1.3W @10GHz) and the good agreement with the simulation.

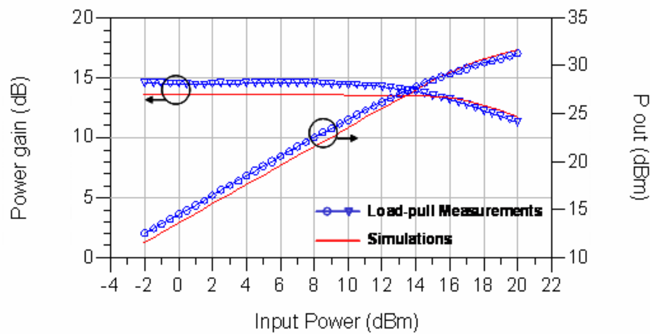

Figure 9. Comparison @10GHz between simulated and measured large signal results for the cascode cell.

The output load was tuned for maximum output power matching at this frequency. The output load impedance for maximum output power of the cascode cell is (20+j12) at a bias level of V_{BIAS_D}=30V, V_{BIAS_G1}=-6V and V_{BIAS_G2}=9V.

V. CONCLUSION

Using an accurate modeling process and power design criteria, an optimized GaN cascode cell has been designed for 4-18GHz power distributed amplifier. Stability analyses were conducted to avoid the occurrence of parametric oscillation phenomena. Furthermore, power simulations were compared to pulsed power measurements. A strong attention must be paid to thermal management. This paper demonstrated that the cascode cell is well suited to the power optimization of distributed architecture over wide bandwidths since it enables higher gain and high power as well as easier output power matching. This result is important for the next generation of high power distributed amplifiers in GaN technology.

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