Design method of balanced AlGaN/GaN HEMT cascode cells for wideband distributed power amplifiers

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Abstract – A specific design of a GaN HEMT cascode cell dedicated to flip-chip distributed power amplifiers is presented in this paper. The active device used in the design is a 8x50μm AlGaN/GaN HEMT grown on SiC substrate. The GaN-based die which integrates the active cascode cell and its passive matching elements is flip-chipped onto an AlN substrate via electrical and mechanical bumps. The matching elements of the cascode cell are composed of series capacitors on the gate of both transistors with additional resistors to insure stability and bias path. The series capacitor on the gate of the 1^{st} transistor is added to enable the power optimization of wideband distributed amplifiers up to their maximum frequency while the series capacitor on the gate of the 2^{nd} transistor is dedicated to the intrinsic power balance of the cascode cell.

Index Terms – Gallium nitride, HEMTs, Balanced cascode cell, Distributed amplifier, Power amplifier, Flip-chip.

I. Introduction

AlGaN/GaN high electron-mobility transistors (HEMTs) have excellent capabilities for power applications up to microwave frequencies because of their large electron velocity ($>10^7$ cm/s), wide-bandgap (3.4eV), high breakdown voltage ($>$ 50 V for $ft = 50$ GHz) and sheet carrier concentration (ηs$>10^{13}$ cm^{-2}). Due to their excellent material properties, AlGaN/GaN HEMTs have famous abilities such as high power, high efficiency and high gain associated to high voltage operation. Especially their high power performances is suitable for radar applications for which they are promising candidates for high power wideband solid-state amplifiers [1], [2]. The best power performances have been demonstrated on SiC substrates mainly due to its higher thermal conductivity (3.5W.cm^{-1}.K^{-1}) and better crystallographic match with the GaN material: power densities as high as 40W/mm @ 4GHz [3] as well as output power of 800W @ 2.9GHz [4] have already been achieved.

This paper deals with the design for power optimization of GaN HEMT cascode cell to be integrated in optimized distributed power amplifiers operating in the 4-18GHz frequency band [5].

Considering the high objectives in terms of power level for the distributed amplifiers, a strong attention has been paid to the thermal management of power devices. Therefore, a flip-chip mounting has been considered in this study onto an aluminum nitride flip-chip substrate (AlN) presenting a high thermal conductivity (180W.m^{-1}.K^{-1}).

II. GaN technology

The selected device is a coplanar AlGaN/GaN HEMT processed on a silicon carbide wafer on which a thin film of gallium nitride has been grown by metal organic vapour deposition (MOCVD) technique. The active device selected for wideband operation up to 18GHz is a 0.15μm gate-length HEMT with a total gate width of 400μm (8x50μm). On-wafer pulsed I-V and pulsed S-parameters measurements have been performed on several samples to derive the nonlinear models for power amplifier design [6]. The nonlinear model is based on modified Tajima equations and 2D splines. This model integrates two source ports because the grounding of the 1^{st} device of the cascode cell (common source) is performed on both sides of its source area through vias connected on the AlN flip-chip substrate. Moreover, the drain pad of the 1^{st} transistor is connected to both sides of the source area of the 2^{nd} transistor (common gate) using a specific metallization path. These models have been implemented in a commercial simulation environment in order to design the optimum power cascode cell.

III. Cascode cell theory

The ideal power cell for wideband distributed operation must display these features:

- a high gain
- a good input-output isolation to reduce the feedback effect
- a weak input resistor
- a high output impedance

The main disadvantage of HEMTs with short gate lengths for millimetre wave bandwidth is to present a low output impedance. However, the main advantage of the cascode cell is to increase (ideally double) the output impedance of a single device. Moreover, the output voltage of a cascode cell is equal to the sum of output voltages of each active cell. Consequently, the cascode cell obviously presents a

Received September 30th, 2007. Revised January 18th, 2008.

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higher gain than a common source transistor and is more attractive for power matching.
Referring to the small signal equivalent model of a classical unoptimized cascode cell (Figure 1.a), the output resistance of the cascode cell is:

$$R_{out} = (\mu + 2) \cdot R_{ds2} \quad \text{with} \quad \mu = gm \cdot R_{ds2} \tag{1}$$

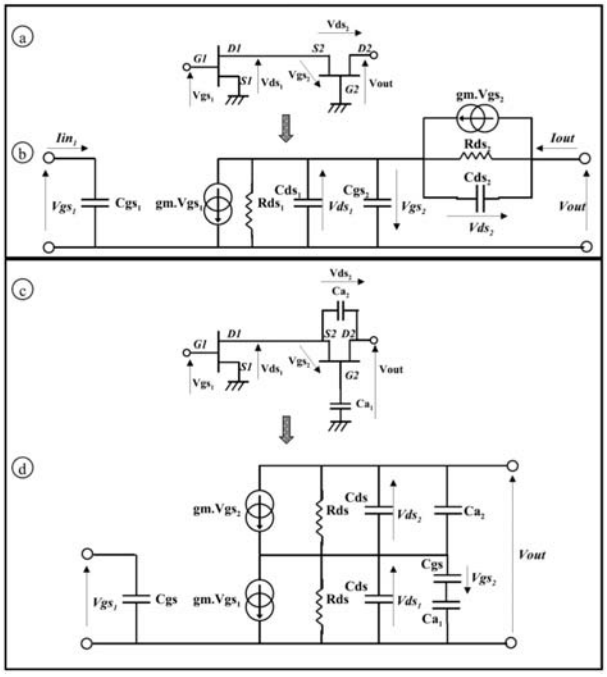

Fig. 1. Schematic of the theoretical cascode cell and the balanced cascode cell with the additive capacitors : Ca_1 and Ca_2.

However, the theoretical configuration of the cascode cell does not allow an optimal power operation. To be power optimized, the cascode cell must integrate an additional series capacitor Ca_1 on the gate of the 2^{nd} transistor (common gate) in order to avoid its early power saturation compared to the 1^{st} transistor (common source). This configuration will be developed in the following paragraph considering that it was retained for our application.
On the other hand, the addition of a Ca_2 capacitor between the drain and the source of the 2^{nd} transistor makes it possible to obtain twice the output conductance of a single common source transistor. It enables to equalize the output impedances of both transistors within the cascode cell by considering that Ca_2 meets the following requirement:

$$Ca_2 = \frac{Cgs \cdot Ca_1}{Cgs + Ca_1} \tag{2}$$

It results that under optimum load conditions, the output voltage of the cascode cell is twice that of a common source transistor. So the output power of the balanced cascode configuration $Pout_{cas}$ is twice that of a common source device $Pout_{tr\_cs}$. Actually:

$$Pout_{cas} = \frac{1}{2} \cdot \Re e \left[(Vds_1 + Vds_2) \cdot \left(gm \cdot \frac{1}{2} \cdot (Vgs_1 + Vgs_2) + \frac{Vds_1 + Vds_2}{2 \cdot Z} \right) \right] \tag{3}$$

where in the optimum power case:

$$\begin{cases} Vgs_1 = Vgs_2 = Vgs_{opt} \\ Vds_1 = Vds_2 = Vds_{opt} \end{cases} \tag{4}$$

and

$$Z = \left(\frac{1}{Rds} + j \cdot \omega \cdot (Cds + Ca_2) \right)^{-1} \tag{5}$$

so that:

(6)

$$Pout_{cas} = \frac{1}{2} \cdot \Re e \left[2 \cdot Vds_{opt} \cdot \left(gm \cdot Vgs_{opt} + \frac{Vds_{opt}}{Z} \right) \right] = 2 \cdot Pout_{tr\_cs}$$

Nevertheless, in most cases, the Ca_2 capacitor could not be integrated because of its low value. The low value of Ca_2 and layout constraints lead to a long-length line connecting drain and source pads of the 2^{nd} transistor inducing parasitic inductance effects. However it allows all the same to highlight the cascode cell relevance for power optimization.

IV. Balanced cascode cell on GaN die

The cascode cell reported in this paper is dedicated to the design and optimization up to 18GHz of flip-chip distributed power amplifiers based on GaN HEMT technology [5].
At first, the design procedure of the distributed power architecture requires to optimize the power performance of the cascode cell on the required bandwidth up to 18GHz [7], [8]. Indeed, the cascode configuration enables to ideally sum the output voltage Vds of each transistor at the same drain current so that to obtain twice the output power of a single transistor. Unfortunately, a classical cascode cell does not meet these requirements as it was previously demonstrated because the input voltage of the 2^{nd} transistor (Vgs_2) limits the output voltage swing (Vds_1) of the 1^{st} transistor (Figure 1.a). To solve this problem, an additional series capacitor Ca_1 is placed on the gate of the 2^{nd} transistor T2 with the main purpose to fix the power matching between transistors (Figure 1.c) independently of frequency.
This capacitor Ca_{1opt} and the input capacitance Cgs of the second transistor act as a frequency independent tension divider between Vds_1 and Vgs_2.

$$Vgs_2 = -\left(\frac{Ca_1}{Ca_1 + Cgs} \right) \cdot Vds_1 \tag{7}$$

$$Ca_{1opt} = \frac{Cgs}{\left(\left|\frac{Vds_{1opt}}{Vgs_{2opt}}\right| - 1\right)} \tag{8}$$

The initial capacitor value of Ca_1 (8) is then optimized under large signal conditions using nonlinear simulations of the balanced cascode cell close to 1dB compression in order to synthesize the required ratio between the optimum large signal control voltages Vds_{1opt} and Vgs_{2opt}.
Meeting the layout constraints, this method has been applied to design the layout of an optimized balanced cascode cell integrating two (8x50μm) GaN HEMTs whose schematic and photograph are respectively shown on Figure 2 and Figure 3.

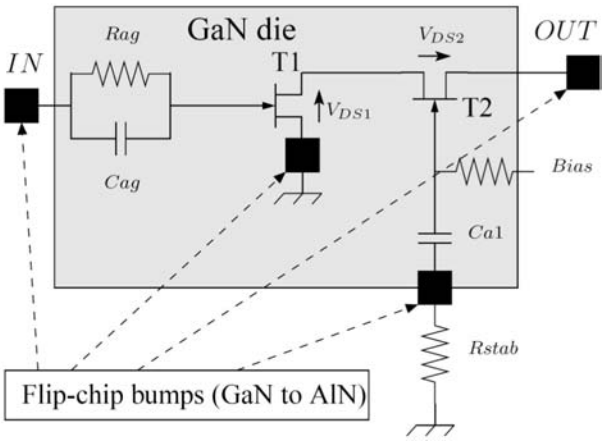

Fig. 2. Schematic of the power cascode cell (GaN die flip-chipped onto AlN).

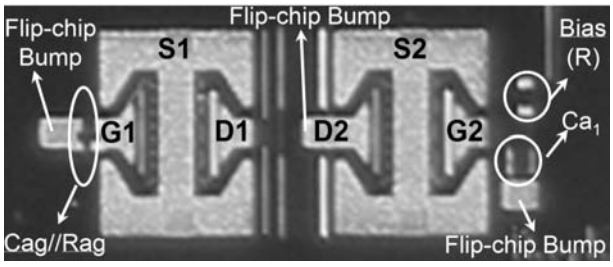

Fig. 3. Photograph of the GaN cascode cell.

Furthermore, for a better transfer from transistor T1 to transistor T2, the drain pad D1 of T1 is directly connected to both part of the source metallization S2 of T2. The gate pad of transistor T1 is grounded onto the flip-chip AlN substrate through its air-bridge playing the role of an electrical bump. The optimum balance capacitor Ca_{1opt} (0.19pF) is integrated on the GaN die in series with the gate G2 of T2 and connected to the flip-chip AlN substrate through an electrical bump. An additional metallic resistor Rstab of 15Ω is added in series with Ca_1 but integrated onto the flip-chip AlN substrate. This resistance is required to stabilize the cascode cell which is known to be very prone to oscillations. In addition with Rollet criterion, the Figure 4 shows the simulated normalized determinant function (NDF) checking the intrinsic stability of the active cascode cell [9]. To implement such a necessary stability analysis, the electrical device models have been modified to enable the open loop analysis [9]. The stability of the cascode cell is one of the most important design issues for power optimization. Figure 4 demonstrates the importance of Rstab for the stabilization at high frequency (e.g. 25GHz).

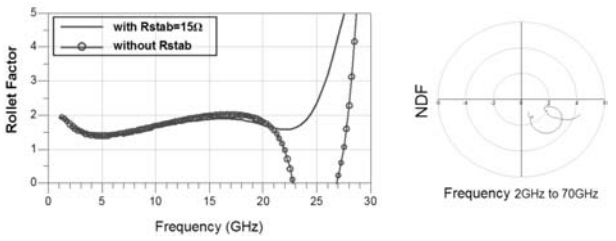

Fig. 4. Influence of Rstab on Rollet factor and NDF of the cascode cell.

Once the power balance of the cascode cell has been optimized by the addition of Ca_1 and its intrinsic stability ensured by the addition of $Rstab$, the cascode cell has to be optimized for wideband power operation within a distributed amplifier. Given the required maximum frequency f_{max} for the distributed amplifier, it is essential to adopt a capacitively coupled distributed architecture [10] in order to meet the requirements of 50Ω input matching and maximum cut-off frequency f_{cg} of the artificial input gate line. Therefore, the capacitive coupling has been integrated on the GaN cascode cell by adding a series capacitance Cag of 0.3pF on the gate G1 of T1 to reach an acceptable equivalent capacitance of the distributed gate line Cgs_{eq} meeting the following constraint on f_{cg} :

$$\begin{aligned} fcg &= \frac{1}{\pi \cdot 50 \cdot Cgs_{eq}} \\ &= \frac{1}{\pi \cdot 50 \cdot \left(\frac{Cag \cdot Cgs}{Cag + Cgs}\right)} > f_{max} \end{aligned} \tag{9}$$

with:

$$Cgs_{eq} = \frac{Cag \cdot Cgs}{Cag + Cgs} \tag{10}$$

In our case, the MIM capacitor Cag of the balanced cascode cell was optimized to enable the design of distributed power amplifiers up to a maximum frequency f_{max} of 18GHz.
Moreover, even if the input voltage division due to Cag in series with Cgs leads to a decreased linear gain of the cascode cell, it makes possible an easier power matching within the distributed architecture up to the maximum frequency f_{max} of the bandwidth. Indeed, the disparity in value of the equivalent input/output capacitances (Cgs_{eq} (10), Cds_{eq} (11)) is reduced so that identical propagation constants of the artificial gate and drain lines within a distributed architecture of such cascode cells can be obtained

by means of weak values of inductances [10].

$$Cds_{eq} \approx 2 \cdot Cds \tag{11}$$

The series capacitors Cag dedicated to coupling the cascode cell to the artificial gate line of a distributed amplifier are shunted by implanted resistors Rag of 500Ω in order to supply the gate bias path since there is no DC gate current flowing through the transistors. Figure 3 shows a photograph of the GaN die integrating the cascode cell and its capacitive and resistive matching elements.

V. Passive part on the flip-chip AIN substrate

A specific AlN die has been designed to separately test the balanced cascode cell.
The AlN die integrates the stability resistance Rstab and the gate bias pads of the 2^{nd} transistor (V_{BIAS_G2}). The gate bias of the 1^{st} transistor (V_{BIAS_G1}) and the drain bias (V_{BIAS_D}) are supplied by the on-wafer probes. Notice that the drain bias voltage V_{BIAS_D} is twice the bias level of a single transistor.
The flip-chip AlN circuit also integrates all the via-holes that permit to ground transistors and matching elements. The dimensions of the AlN chip are less than (2.5x1.7)mm^2. Figure 5.a shows a photograph of the AlN die designed to flip-chip the GaN cascode cell while Figure 5.b shows a photograph of two GaN cascode cells flip-chipped onto the AlN substrate with the external SMC decoupling capacitors.

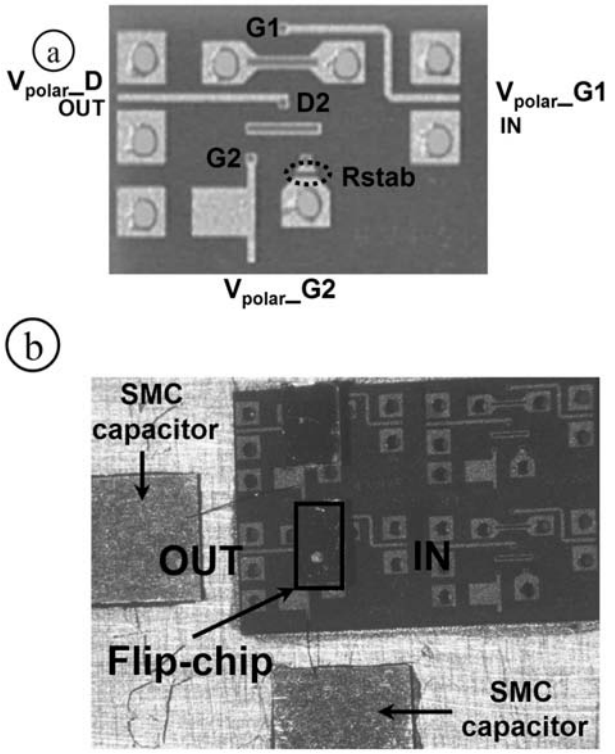

Fig. 5. Photograph of : (a) the AlN die designed to flip-chip the GaN cascode cell (Input and output lines, DC bias paths, Electrical bumps, Via-holes) and (b) two GaN cascode cells flip-chipped onto AlN substrate for on-wafer measurements.

VI. Simulation results

The design of the cascode cell has been performed with the help of the ADS simulation software.
Figure 6.a shows a comparison of the maximum available gain from 4 to 18GHz between the balanced cascode cell and a single device which also integrates the gate coupling Cag and Rag required by distributed architectures.

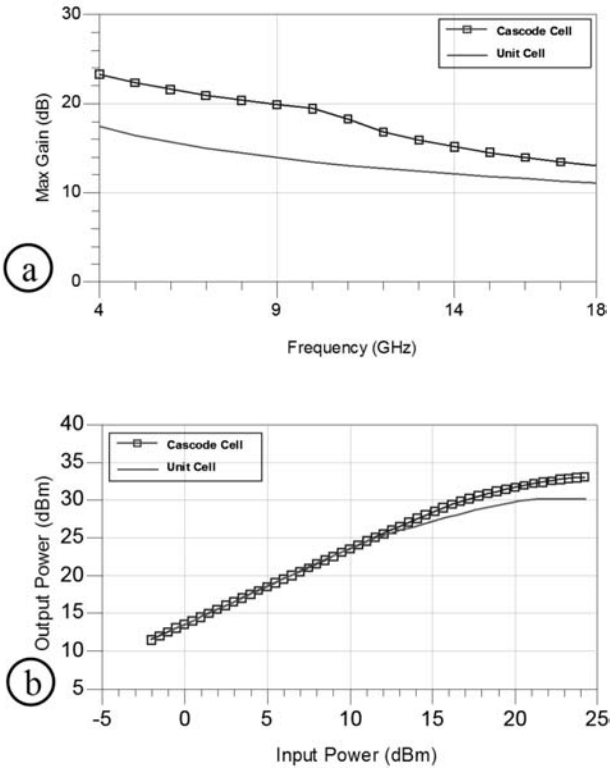

Fig. 6. Comparison of maximum available gain on 4-18GHz (a) and power characteristics at 10GHz (b) between the balanced cascode cell and a single transistor with input (Cag // Rag) cell.

As expected, the balanced cascode cell enables to reach higher gain from the beginning of the bandwidth up to the maximum frequency at 18GHz. In the same conditions, Figure 6.b shows the comparison of the power characteristics at 10GHz of the balanced cascode cell compared to the single device demonstrating that the cascode cell enables higher output power.
In order to check the power optimization of the cascode cell, Figure 7 shows the simulated intrinsic load lines of the two transistors T1 and T2 of the cascode cell at 10GHz in the same load conditions as those used for the load-pull power measurements reported in the next section.

VII. Measurements

A) Scattering parameters measurements

In order to check the accuracy of the linear and nonlinear modelling of the balanced cascode cell, on-wafer S-

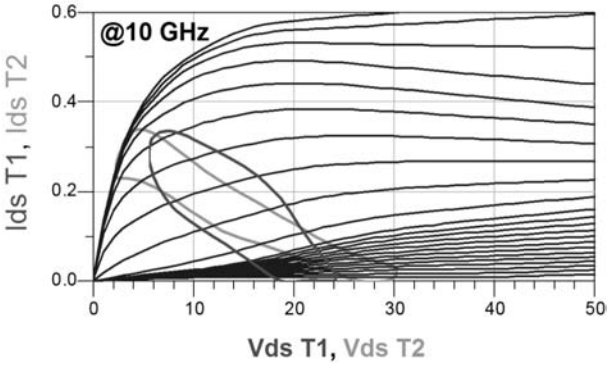

Fig. 7. Intrinsic load lines of each transistor of the cascode cell @ 10GHz.

parameters measurements have been performed in the 0.5-20GHz bandwidth as shown on Figure 8.a. The comparison of simulated and measured S-parameters demonstrates a good agreement. It is interesting to note that the gain of the balanced cascode cell is quite flat in the beginning of bandwidth while it is not true for a single transistor.

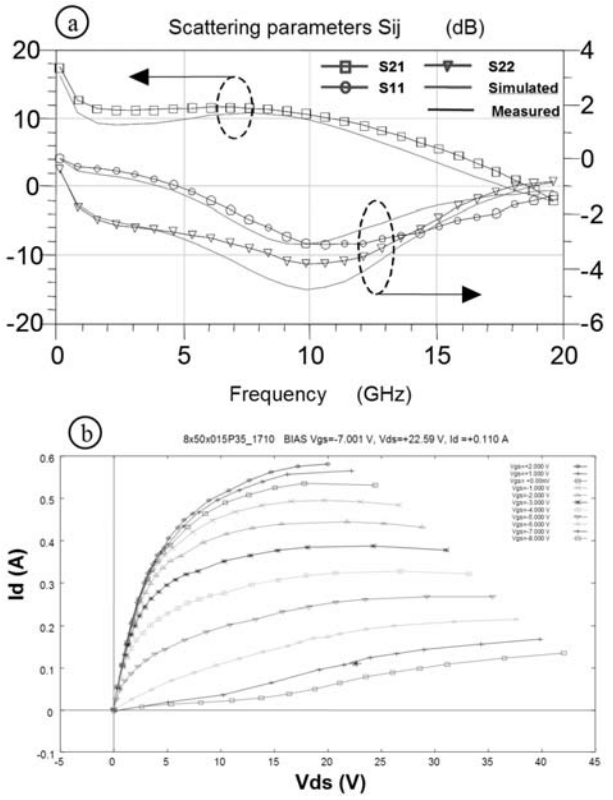

Fig. 8. (a) : Simulated and measured S-parameters of the cascode cell. (b) : Pulsed I-V Characteristic of 8x50μm device measured at the quiescent bias point ($Vgs0$=-7V, $Vds0$=22.6V).

B) Pulsed I-V and pulsed load-pull measurements

1) Pulsed I-V measurements

Pulsed I-V measurements have been performed on the 8x50μm HEMT device up to 45V of Vds. A drain current density of 1.45 A/mm is obtained at the quiescent bias point (Vgs_0=-7V, Vds_0=22.6V). The kink effect at pinch-off voltage can be observed on Figure 8.b which is one of the critical effect that decrease power performances.

On-wafer pulsed Load-pull measurements of the cascode cell have been performed in order to check and compare the optimum power state derived from nonlinear simulations with power measurements. During the power load-pull characterization, the pulses were 10μs width according to a 10% duty cycle. Both RF signals and biases were pulsed.

2) Load-pull measurements setup

The load-pull measurement setup is based on the use of a VNA including a receiver mode test-set which enables pulsed signal measurements. The synoptic of this pulsed measurement setup is shown on Figure 9. The calibration of this system includes both a relative calibration such as SOLT or LRM method and a power calibration in order to measure the four absolute waves (a1, b1, a2 and b2) at the fundamental frequency at the calibration reference plane (the tip of the probes).

In order to be self consistent, the bench calibration procedure uses the same pulsed CW signal which is on use during the measurements. Both RF and DC value are measured into the pulse width [11].

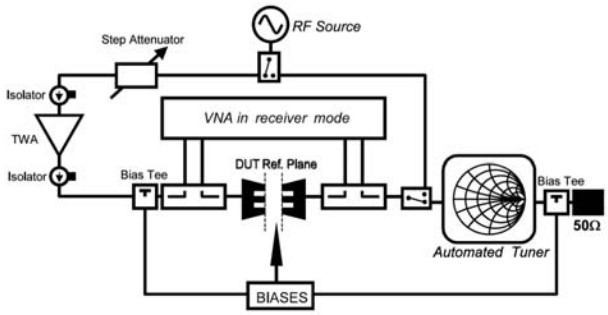

Fig. 9. On-wafer Pulsed Load-Pull Measurement Setup.

3) Load-pull measurements results

Figure 10 shows the comparison between nonlinear simulations and load pull power measurements of the balanced cascode cell at 10GHz. The output load was tuned for

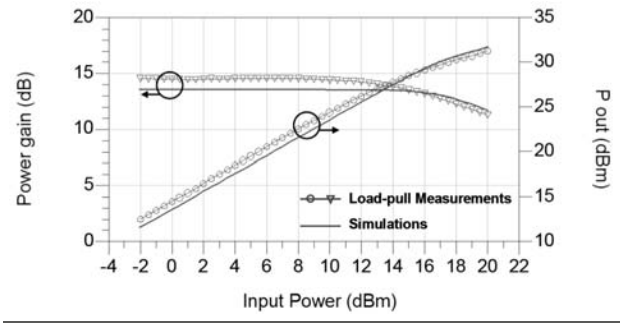

Fig. 10. Comparison between simulated and measured large signal results for the cascode cell @ 10GHz.

maximum output power matching at this frequency. The optimum load impedance for maximum output power of the cascode cell is (20+j.12) at a bias level of V_{BIAS_D}=30V, V_{BIAS_G1}=-6V and V_{BIAS_G2}=9V.
A very good agreement is obtained between power measurements and simulations even if a small shift of 1dB is observed on the small signal gain where the nonlinear model is pessimistic. The balanced cascode cell integrating the gate coupling capacitors yields 1.3W output power at 10GHz.

VIII. Conclusion

The design method of a power balanced GaN cascode cell has been reported for the wideband power optimization of capacitively coupled distributed amplifiers. After the flip-chip mounting of the balanced GaN cascode onto AlN substrate, pulsed S-parameters measurements and power measurements were compared to nonlinear simulations based on a specific nonlinear electrothermal model [12]. The cascode cell designed onto the GaN chip integrates specific passive matching elements such as the series MIM capacitors (Ca_1, Cag) on the gate of each transistor to ensure the optimum power balance over wide bandwidths up to 18GHz. Additional resistors (Rag, $Rstab$) are necessary for ensuring the DC bias and the stability. This paper demonstrates that the cascode cell is well suited to the power optimization of distributed architectures over very wide bandwidths since its enables higher gain and high power as well as easier output power matching since its optimum power load is twice the optimum load of a single device.

Acknowledgements

The authors wish to acknowledge TIGER laboratory for epitaxial layers and processing on SiC wafers.

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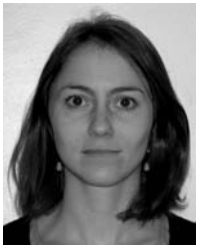

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