Balanced AlGaN/GaN HEMT cascode cells : design method for wideband distributed amplifiers

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A report is presented on the specific design of a GaN HEMT cascode cell demonstrating significant improvement for flip-chip distributed power amplifiers. The active device is a 8 × 50 μm AlGaN/GaN HEMT grown on SiC substrate. The GaN-based wafer integrating the active part is flip-chipped onto an AlN substrate via electrical and mechanical bumps. The cascode cell integrates matching elements for power optimisation of wideband distributed amplifiers up to their maximum frequency and for intrinsic power balance of the cascode cell. Additional resistors are integrated to ensure bias path and stability, this last one being decisive for the studied application.

Introduction: AlGaN/GaN HEMTs have attracted much research interest owing to their inherent advantages of high voltage operation and high power density. The best power performances have been demonstrated on SiC substrates; power densities as high as 40 W/mm at 4 GHz [1] as well as output power of 800 W at 2.9 GHz [2] have been achieved. The AlGaN/GaN device appears as the leading candidate for wideband power amplifiers [3, 4]. In this context, this Letter deals with the design of GaN HEMT cascode cells to be integrated in optimised distributed power amplifiers operating in the 4 to 18 GHz frequency band [5].

GaN technology: In this study, the coplanar AlGaN/GaN HEMT is processed on a silicon carbide wafer on which a thin film of gallium nitride has been grown by metal organic vapour deposition (MOCVD) technique. The active device selected for wideband operation up to 18 GHz is a 400 μm HEMT (8 × 50 μm). On-wafer pulsed I-V and S-parameter measurements have been performed to derive the nonlinear models. A drain current density of 1.45 A/mm is obtained at the quiescent bias point ($Vgs_0 = -7$ V, $Vds_0 = 23$ V). These models are based on modified Tajima equations and splines [6]. They have been implemented in a commercial simulation environment in order to design the optimum power cascode cell.

Balanced cascode cell on GaN die flip-chipped onto AlN substrate: The power performance of the cascode cell is one of the most important design issues in designing distributed power architectures on the required bandwidth up to 18 GHz [7]. In fact, the cascode configuration allows one to ideally sum the output voltage Vds of each transistor at the same drain current in order to obtain twice the output power of a single transistor. Unfortunately, the input voltage of the second transistor (Vgs_2) restricts the output voltage swing (Vds_1) of the first transistor in a classical cascode configuration. To overcome this problem, an additional series capacitor Ca_1 is placed on the gate of the second transistor, the main objective being to fix the power matching between transistors independently of frequency (Fig. 1). This capacitor Ca_{1opt} and the input capacitance Cgs of the second transistor act as a frequency independent tension divider between Vds_1 and Vgs_2:

$$Ca_{1opt} = \frac{Cgs}{\left(\left|\frac{Vds_{1opt}}{Vgs_{2opt}}\right| - 1\right)}$$

Using nonlinear simulations of the balanced cascode cell close to 1 dB compression, this initial capacitor value of Ca_1 is optimised so as to synthesise the required ratio between the optimum large signal control voltages Vds_{1opt} and Vgs_{2opt}. As shown in Fig. 1, the GaN die integrates the optimum balance capacitor Ca_{1opt} (0.19 pF) in series with the gate G2 of T2 which is connected to the flip-chip AlN substrate through an electrical bump. In series with Ca_1, an additional metallic resistor Rstab of 15 Ω is added and integrated onto the flip-chip AlN substrate. The cascode cell is known to be very prone to oscillations, therefore this resistance is required. In addition with Rollet criterion, Fig. 2 shows the simulated normalised determinant function (NDF) checking the intrinsic stability of the active cascode cell [8]. It demonstrates the importance of Rstab for the stability at high frequency (e.g. 25 GHz). The cascode cell stability is a fundamental issue for the power optimisation. Besides, the optimisation for wideband power operation within a distributed amplifier is required. A capacitively coupled distributed architecture [9] is essential in order to meet the requirements of 50 Ω input matching and maximum cutoff frequency f_{cg} of the artificial input gate line given the main maximum frequency f_{max} for the distributed amplifier. Consequently, the capacitive coupling has been integrated by adding a series capacitance Cag (0.3 pF) on the gate G1 of the first transistor on the GaN die. Furthermore, convenient power matching is obtain within the distributed architecture up to the maximum frequency f_{max} (18 GHz) of the bandwidth in spite of the input voltage division due to Cag in series with Cgs which leads to a decreased linear gain of the cascode cell. These series capacitors Cag are shunted by implanted resistors Rag of 500 Ω in order to supply the gate bias path since there is no DC gate current flowing through the transistor (Fig. 3*a*). The ALN die (Fig. 3*b*) integrates the stability resistance Rstab, via-holes and the gate bias pads of T2 (V_{BIAS_G2}). The gate bias of the first transistor (V_{BIAS_G1}) and the drain bias (V_{BIAS_D}) are supplied by the on-wafer probes. The drain bias voltage V_{BIAS_D} is twice the bias level of a single transistor.

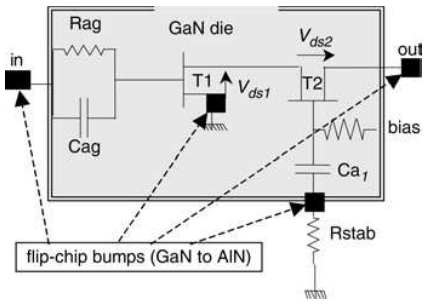

Fig. 1 *Schematic of power cascode cell (GaN die flip-chipped onto AlN)*

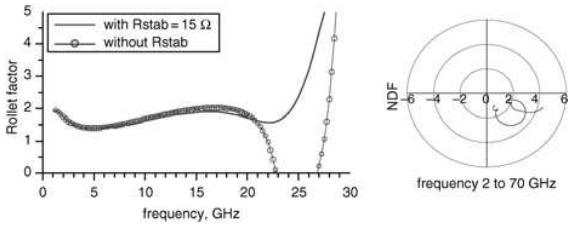

Fig. 2 *Influence of Rstab on Rollet factor and NDF of cascode cell*

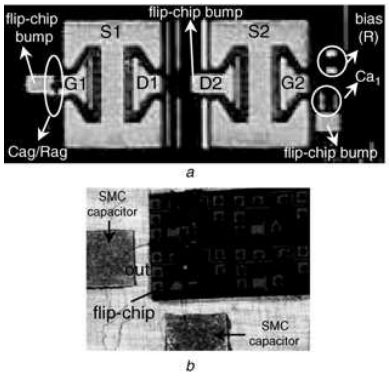

Fig. 3 *Photographs of GaN cascode cell (Fig. 3a) and of two GaN cascode cells flip-chipped onto AlN substrate for on-wafer measurements (Fig. 3b)*

Measurements results: To check the accuracy of the linear and nonlinear modelling of the balanced cascode cell, on-wafer S-parameter measurements were carried out in the 0.5 to 20 GHz bandwidth as shown in Fig. 4*a*. Comparison of simulated and measured S-parameters demonstrates good agreement. It is interesting to note that the gain of the balanced cascode cell is quite flat in the beginning of bandwidth while not true for a single transistor. Furthermore, on-wafer pulsed load-pull measurements have been performed to check and compare the optimum power state derived from nonlinear simulations with power measurements. Both RF signals and biases were pulsed. Fig. 4*b* shows comparison between nonlinear simulations and

load-pull power measurements of the balanced cascode cell at 10 GHz. The optimum load impedance for maximum output power of the cascode cell is (20 + j.12) at a bias level of $V_{BIAS\_D} = 30$ V, $V_{BIAS\_G1} = -6$ V and $V_{BIAS\_G2} = 9$ V. Very good agreement is obtained between power measurements and simulations even if a small shift of 1 dB is observed on the small signal gain where the nonlinear model is pessimistic. The balanced cascode cell integrating the gate coupling capacitors yields 1.3 W output power at 10 GHz.

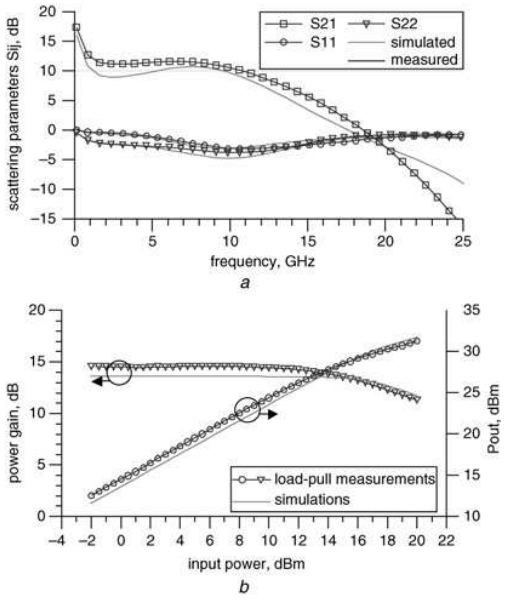

Fig. 4 *Comparison between simulated and measured S-parameters of cascode cell at $V_{BIAS\_D} = 30$ V, $V_{BIAS\_G1} = -6$ V, $V_{BIAS\_G2} = 9$ V (Fig. 4a) and comparison between simulated and measured power results for cascode cell at 10 GHz (Fig. 4b)*

Conclusion: A power balanced GaN cascode cell designed for capacitively coupled wideband power distributed amplifiers is presented. The cascode cell integrates specific passive matching elements to ensure the optimum power balance over wide bandwidths up to 18 GHz thanks to series MIM capacitors Ca_1 and Cag on the gate of each transistor and to ensure DC bias and stability thanks to additional resistors Rag and Rstab. The balanced GaN cascode cell is flip-chipped onto an AlN substrate for which dimensions are less than (2.5×1.7) mm^2. Pulsed S-parameters and power measurements were performed and compared with nonlinear simulations based on a specific nonlinear electrothermal model. Experimental results confirm that the cascode cell is an effective topology to use in distributed architectures over very wide bandwidths. Optimum cascode power load is twice the optimum load of a single device, giving it higher gain and higher power.

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