

An Experimental Study for the Design of Dual Input Load Modulated Wideband GaN Amplifier

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Abstract—In this paper, we present an experimental study focused on the characterization of a dual input Doherty Power Amplifier (DPA). A calibrated set-up is used for an accurate characterization of a DPA demonstrator and the study of several input driving conditions. A demonstrator PA which uses two packaged 10-W GaN HEMT from Wolfspeed was fabricated. Measurements obtained for several driving conditions (power levels and relative phase differences) show Drain Efficiency (DE) performances of $DE \approx 55\%$ at 6-dB Output Back Off (OBO) and $DE \approx 60\%$ at 20-W saturated power over a 2.1-2.6 GHz bandwidth. The main focus of the paper concerns the trade-off between efficiency and power gain shape versus output power that can be obtained with dual input architectures and input signal driving conditions.

Keywords—Doherty, GaN, power amplifiers, dual input, digitally assisted

I. INTRODUCTION

The DPA is a well known architecture providing a high average efficiency over a large OBO. Its success comes from its ease of implementation as well as its effectiveness in presence of modulated signals with high Peak to Average Power Ratio (PAPR). However, this architecture suffers from inherent bandwidth limitations due to the need of an impedance inverting function and a quite complicated output power combining circuit. Furthermore, Doherty amplifiers have a non symmetrical architecture that put many circuit design constraints to reach high efficiency and wideband operation at both back-off and saturated power conditions. In this context, wideband and high efficiency DPA design strategy has known many researches over the past few years and many DPA demonstrators taking benefit of high power and broadband capabilities of GaN technology have been reported.

Generally speaking, DPA design strategy consists of a two-point wideband output matching ensuring smooth, small and uniform variations of real and imaginary parts of admittances presented to intrinsic drain current sources of main and auxiliary transistors, along with minimal group delay of matching circuits from the input up to the common output combining node. Moreover, the DPA impedance inverter design should include the effect of transistor's parasitics for bandwidth improvements.

Jointly to circuit design improvements, the dual-input Doherty approach reported in [1], [2], [3], [4], [5] can offer additional degrees of freedom and flexibility for the design of high efficiency and linear DPAs. Digitally assisted power

amplifiers can reveal to be attractive in future emitter front ends thanks to current enhancements on digital signal processors.

In part II of the paper, a 20-W S-Band dual input DPA demonstrator is presented. The design methodology, inspired by several previous reported works ([6], [7], [8]) is described. Then, part III proposes a two channel calibrated test bench that provides a very attractive interest for the optimization of high efficiency and linear load modulated power amplifiers. Finally in section IV, measurement results are presented and highlight the interest of this work in the framework of linear and high efficiency load modulated power amplifiers design.

II. DPA DEMONSTRATOR

The topology of the DPA demonstrator is illustrated in figure 2. We will discuss the main design steps and present the fabricated dual input Doherty demonstrator. Although it is not the main aspect of this work, some crucial points are worth noting for a wideband design process and a dual input experimental study.

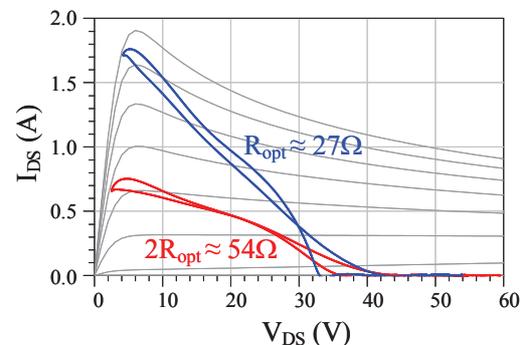


Fig. 1. Simulated loadlines at 2.5 GHz on CGH40010F transistor at a 6-dB OBO power level (red) and peak output power (blue).

A. DPA Design Methodology

The design of the output power combining network of a DPA is one of the major difficulty encountered to reach high PAE performances at both 6-dB OBO and saturated power over a wide bandwidth. The impedance inverting and matching circuits must include parasitic components of the transistors to get the proper load modulation at intrinsic ports of the drain current sources of the active cells. The common node load resistance (R_L) must be properly chosen as a function of

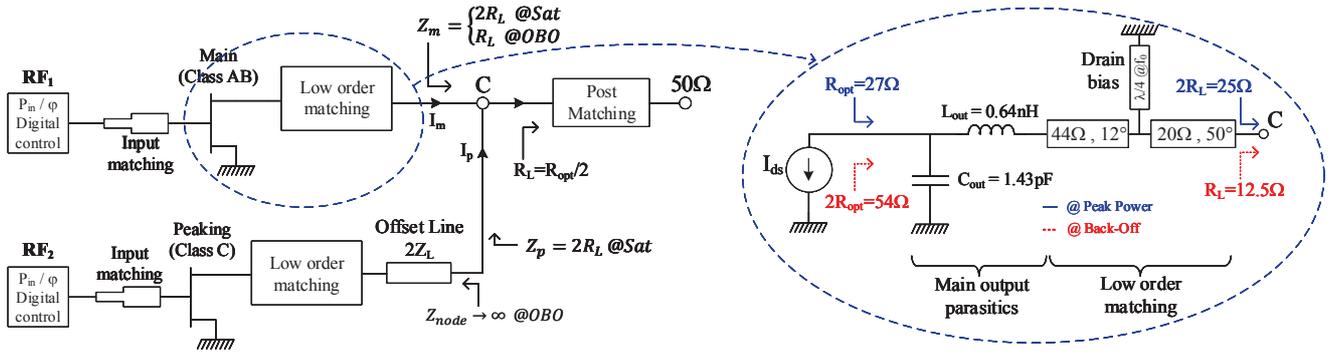


Fig. 2. Proposed post-matching DPA topology using low order matching circuits. By properly tuning characteristic impedances and electrical lengths of the stepped lines according to the output parasitics values, an inverting function can be achieved on a wide bandwidth from the intrinsic plane to the common node C.

optimal load impedance of the main transistor (R_{opt} and $2R_{opt}$ respectively at saturated and OBO power levels).

Using 10-W GaN HEMT CGH40010F transistor's model (provided by Wolfspeed), harmonic loadpull simulations at 2.5 GHz lead to an optimal class-B intrinsic load impedance of $R_{opt}=27\Omega$ at peak power level. As a consequence, an impedance of $2R_{opt}=54\Omega$ must be presented to the main transistor at 6-dB OBO operation of the amplifier (figure 1).

To get a wideband operation and to build a demonstrator for dual-input monitoring study, matching circuits are only realized using stepped line transformers as shown on figure 2. Characteristic impedances and electrical lengths of lines have been optimized in order to satisfy a proper load modulation and to have progressive and smoothly varying impedance transformation ratio from the transistors up to the final 50Ω load.

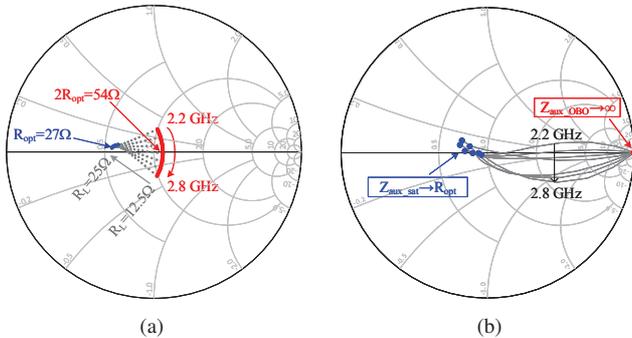


Fig. 3. Simulated load impedances (a) seen by the main current source and (b) by the auxiliary current source at 6-dB OBO power level (red line) and at saturation level (blue line) over the frequency band (2.2-2.8 GHz)

As depicted in figure 2, a simplified equivalent circuit of the main amplifier's output is considered. For simplification, the output impedance at the combining node is represented as a variable resistance, varying from R_L to $2R_L$ as the input power increases. The low order matching circuit combined with the component parasitics performs an appropriate load

modulation (from R_{opt} to $2R_{opt}$) at the intrinsic port of the main transistor's drain current source. In the present case, the value of R_L is set at 12.5Ω to maintain the desired impedance at OBO over the bandwidth. As illustrated in figures 3(a) and 3(b), the matching circuit ensures a real to real impedance inversion on a wide bandwidth and is able to meet the requirements at 6-dB back-off and saturation level.

A Post-Matching Network (PMN) is in our case necessary to optimize the power transfer of the combined signals to the 50Ω load on a wide bandwidth.

At 6-dB OBO a high impedance presented by the peaking branch at the combining node is essential. Otherwise an insufficient impedance value would lead to current leakage from the main cell and would decrease the overall efficiency at OBO. Therefore, an offset line is used in the proposed architecture so as to ensure high impedance condition and a purely real load modulation at the intrinsic plane of the auxiliary transistor.

As far as the input matching circuits are concerned, they also have been designed using stepped lines in order to improve the flexibility for analysis over a wide frequency bandwidth of interest.

B. Fabricated Circuit

A picture of the fabricated DPA is shown on figure 5. It has been fabricated on the RF substrate Rogers 4350B. The main transistor is biased in class AB ($V_{GS0}=-2.85V$) with a quiescent current of 70mA. The auxiliary transistor is biased in class C ($V_{GS0}=-6.2V$) with a pinch-off voltage around $V_p=-3.1V$. Measurements shown in part III are performed with the main amplifier biased at $V_{DS0}=26V$ and the auxiliary amplifier at $V_{DS0}=32V$.

III. CALIBRATED DUAL CHANNEL MEASUREMENT SET-UP

A dedicated test bench has been developed for the characterization of dual-input load modulated amplifiers. It is based on a dual channel Vector Signal Generator (VSG) from Rhode & Schwarz. As illustrated on figure 6, this

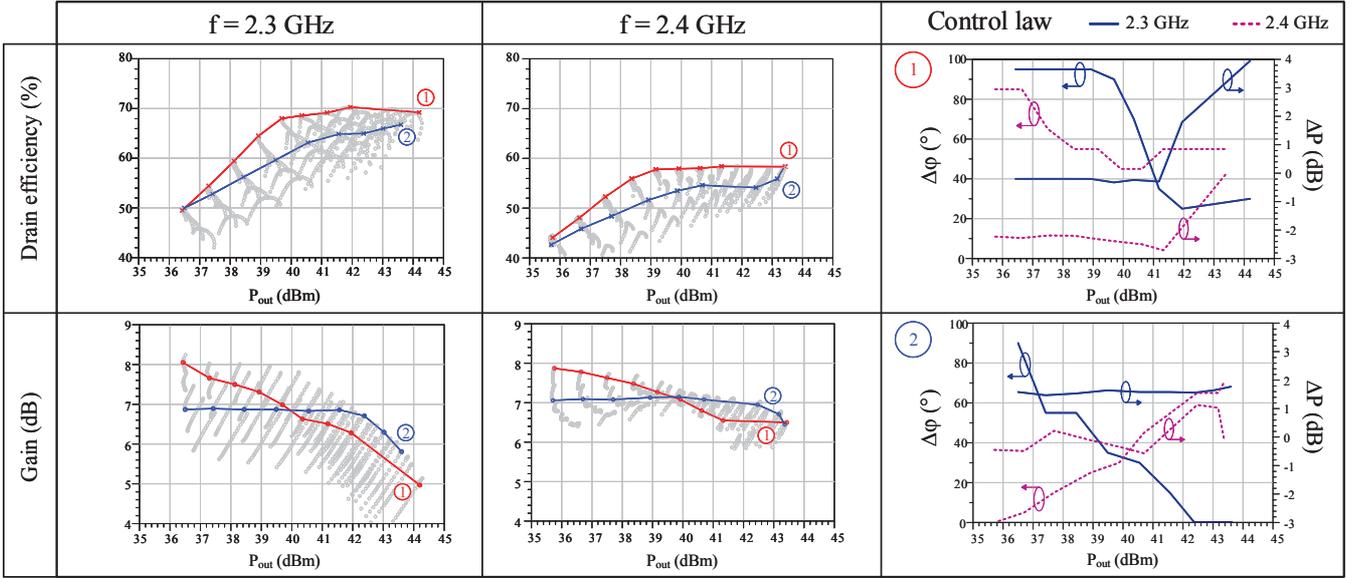


Fig. 4. Measured DE and gain for two driving conditions (case n°1: maximum DE and case n°2: flat gain) and associated amplitude/phase driving conditions.

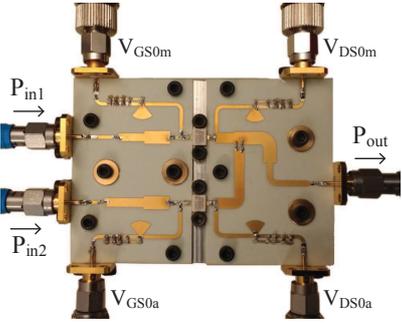


Fig. 5. Designed dual input DPA.

VSG includes DACs synchronously triggered and driving two independent IQ modulators sharing the same Local Oscillator (LO). The CW signals at the output of the VSG are obtained from constant base-band modulation (BB). The system is calibrated at the DUT reference planes. This calibration consists of a power and phase calibration.

First, the power calibration is performed by connecting a power meter at the reference planes. After this step, power meters P_{in1} and P_{in2} measure $|a_1|$ and $|a_2|$.

Secondly, a phase calibration, based on the assumption of linear time group delay in the setup, is performed. It consists of measuring the output power of a pre-characterized power combiner driven by a CW signal at both inputs simultaneously. According to the knowledge of the S3P combiner, the base-band phase offset $\Delta\Phi$, and assuming $\text{Arg}\{a_1\} = 0$, we can deduce $\text{Arg}\{a_2\} = \Delta\varphi$ for any frequency.

Once calibrated, the measurement setup provides $|a_1|$, $|a_2|$ and $\Delta\varphi$. In the next section, ΔP will be defined as $|a_2|^2/|a_1|^2$ or $P_{Aux\text{ dB}} - P_{Main\text{ dB}}$.

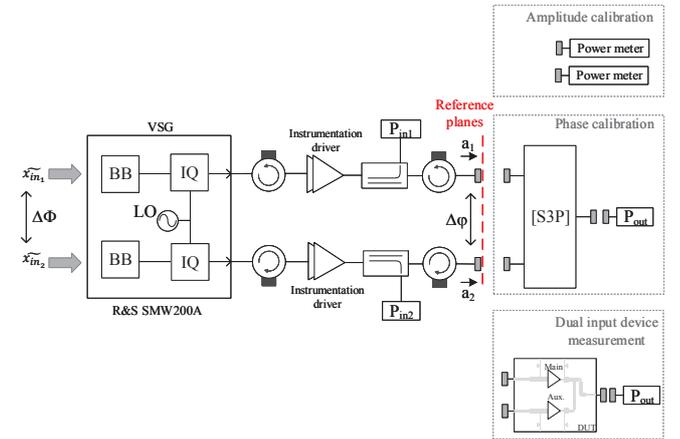


Fig. 6. Experimental calibrated test setup for digitally assisted dual-input amplifiers.

IV. MEASUREMENT RESULTS

Measurement results shown on figure 4 illustrate the effect of the digital control of $\Delta\varphi$ and ΔP on the drain efficiency and the gain. These two performances have been measured for various power balance ΔP and phase differences $\Delta\varphi$ between the inputs of the main and auxiliary PAs.

Two cases are reported: case n°1 with the aim of reaching the maximum achievable drain efficiency and case n°2 to obtain a flat gain as a function of the output power. In both cases, a similar control law on $\Delta\varphi$ (decreasing as the output power increases) can be observed. However a difference can be noticed concerning the power balance. To reach a flat gain, ΔP has to be set at a quasi-constant value around 1.6 dB. At 2.4 GHz, to obtain a better gain flatness (case n°2), it can

be seen that the phase difference increases as a function of P_{out} . On the contrary, in order to ensure a maximum efficiency at OBO, both main and auxiliary have to be driven with the same input power. For output powers higher than 41 dBm, the driving level of the auxiliary amplifier has to be increased in order to perform a larger load modulation while maintaining a high efficiency. In other words, the auxiliary transistor will quickly produce more current to help the load modulation of the main transistor. These two cases bring forward the efficiency-linearity trade-off.

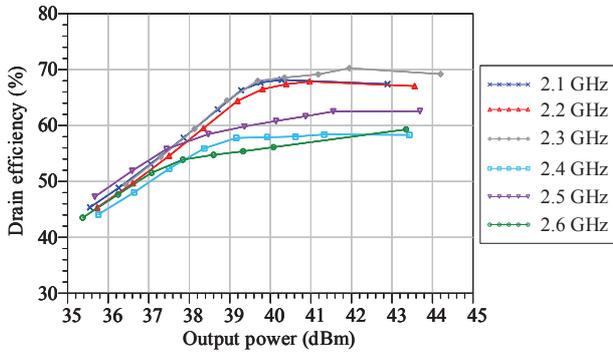


Fig. 7. Measured drain efficiency versus output power of the Doherty PA over 2.1-2.6 GHz. For each frequency, the digital control of ΔP and $\Delta\varphi$ is optimized for maximum efficiency.

Based on the previous observations, the same procedure to reach the maximum efficiency can be extended for multiple frequencies as presented on figure 7. The measured results with digital control at each frequency exhibits good efficiency performances over the band from 2.1 to 2.6 GHz. One can observe that the frequency of operation has been shifted from 2.5 to 2.3 GHz compared to the simulations. As can be seen, the drain efficiency performances remain higher than 50% over 500 MHz at both 38 and 44 dBm output power. The load modulation effect is clearly visible, leading to a high drain efficiency for output power levels higher than 38 dBm. It has been observed that the phase does not have an impact on the efficiency under an output power of 39-38 dBm. This proves the effectiveness of the offset line in the output combiner circuit. It presents an open circuit at the common node and it avoids current leakage of the auxiliary for low power operation.

V. CONCLUSION

A 20W digitally driven DPA using low order matching circuits to realize broadband operation and high OBO efficiency has been presented. It has been shown that an appropriate digital control of the amplitude and the phase of the auxiliary PA can provide a high efficiency at both full output power and OBO over a significant bandwidth compared to a single input Doherty power amplifier. The dual input architecture provides additional degrees of freedom by allowing an adaptive control of the driving signals of the PAs. The fabricated DPA shows above 50% drain efficiency at 6-dB OBO and 60% at peak output power within a 500 MHz bandwidth. This work shows very useful measurement based

results leading to a better knowledge of power dependent vector input splitting which could be implemented with analog predistortion for efficiency-linearity enhancement purpose.

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REFERENCES

- [1] A. Piacibello, R. Quaglia, V. Camarchia, C. Ramella, and M. Pirola, "Dual-Input Driving Strategies for Performance Enhancement of a Doherty Power Amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, June 2018, pp. 1–4.
- [2] M. Masood, P. Rashev, and J. S. Kenney, "Digitally-assisted Doherty Power Amplifier: Efficiency Enhancement and Linearity Improvement," in *IEEE MTT-S Int. Microw. Symp. Dig.*, June 2018, pp. 801–804.
- [3] C. M. Andersson, D. Gustafsson, J. C. Cahuana, R. Hellberg, and C. Fager, "A 1-3-GHz Digitally Controlled Dual-RF Input Power-Amplifier Design Based on a Doherty-Outphasing Continuum Analysis," in *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 10, pp. 3743–3752, October 2013.
- [4] R. Darraji, F. M. Ghannouchi, and O. Hammi, "A Dual-Input Digitally Driven Doherty Amplifier Architecture for Performance Enhancement of Doherty Transmitters," in *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 5, pp. 1284–1293, May 2011.
- [5] R. Quaglia, M. D. Greene, M. J. Poulton, and S. C. Cripps, "Design and Characterization of a 1.7-2.7 GHz Quasi-MMIC Doherty Power Amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2017, pp. 771–773.
- [6] Y. Komatsuzaki, K. Nakatani, S. Shinjo, and S. Miwa, "3.0-3.6 GHz Wideband, over 46% Average Efficiency GaN Doherty Power Amplifier With Frequency Dependency Compensating Circuits," in *Proc. IEEE Power Amplifiers for Wireless Radio Appl. Top. Conf.*, January 2017, pp. 22–24.
- [7] J. Pang, S. He, C. Huang, Z. Dai, J. Peng, and F. You, "A Post-Matching Doherty Power Amplifier Employing Low-Order Impedance Inverters for Broadband Applications," in *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 4061–4071, December 2015.
- [8] R. Giofrè, L. Piazzon, P. Colantonio, and F. Giannini, "A Closed-Form Design Technique for Ultra-Wideband Doherty Power Amplifiers," in *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3414–3424, December 2014.