

X-band 10 W MMIC High-Gain Power Amplifier with up to 60% PAE

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Abstract—This paper describes a power amplifier operating at X-band demonstrating 61% power added efficiency (PAE) at 10 GHz associated with 14 W output power in CW mode. The design uses a 0.15 μ m GaN 3MI process from TriQuint™. The devices operate at a peak power density of 3.8 W/mm at 10 GHz with a PAE higher than 48% over a 500-MHz bandwidth. The two-stage MMIC PA has a saturated gain of 19 dB at peak efficiency. The total size of the chip is 9.2 mm².

Keywords—Power Amplifiers, Gallium Nitride, high efficiency, MMIC, X-band.

I. INTRODUCTION

Wireless systems operating at X-band target applications such as satellite transmitters, atmospheric radar or airborne phased array radar. Although this frequency range has been used for decades, the need for increased efficiency of the solid-state transmitters is still an important goal. For airborne and spaceborne applications, the decrease in power requirements is especially important due to the size and weight of the needed mechanical structure to handle the overall power dissipation.

X-band active electronically scanned array (AESA) technologies have been widely developed in the last two decades to accomplish different missions, such as air-to-air fighter combat, air-to-ground missions or surveillance and tracking [1]. A pulse Doppler X-band phased array requires on the order of 5,000 T/R modules per square meter, making integration a necessity. This in turn requires increasing the PAE, so that the heat sink structure and/or cooling system can be significantly downsized. Recent advances in GaN devices have resulted in a number of high-efficiency high-power integrated amplifiers in the 10-GHz frequency range.

Fig.1 summarizes recent published results for GaN MMIC power amplifiers operating within the range of X-band. The plot details maximum achieved PAE, corresponding output power and measured gain at maximum PAE, indicated by the size of the circle. In addition, some high efficiency results (PAE>60%) have been reported with single-stage 2-3 W PAs having saturated gain less than 10-dB, while the higher-power multi-stage PAs generally have PAE<50%. This paper presents a two-stage, high-power GaN MMIC amplifier exhibiting a peak power of 14 W at PAE = 61% and $G_{sat} = 19$ dB. The PA outputs over 10 W of power in the 10-10.5 GHz bandwidth with a PAE higher than 48%. The reference [2] reported an X-band power amplifier exhibiting similar peak performance using the same process. The design and characterization of this 9.2 mm² MMIC suitable for phased array integration are presented in the remainder of the paper. Note that in some cases,

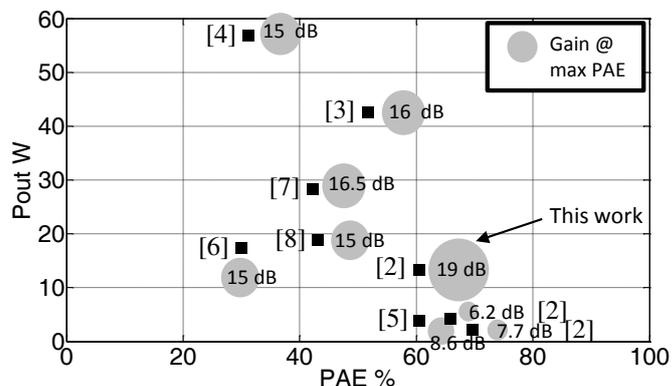


Fig. 1. Recent published power performances of GaN based MMIC X-band power amplifiers. Grey circles highlight the achieved gain at maximum PAE.

the reported results are from on-wafer probed measurements, while in other cases, they include SMA connectors.

II. POWER AMPLIFIER DESIGN

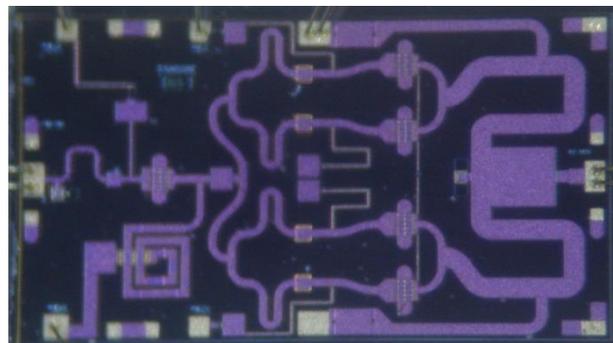


Fig. 2. Photograph of the X band 4 x 2.3 mm² power amplifier fabricated with the 0.15 μ m GaN 3MI process from TriQuint™.

Fig.2 is a photo of the fabricated circuit. The total chip size is 9.2 mm². The electro-thermal nonlinear model was extracted by Modelithics™ using conventional pulsed RF/IV and CW load pull measurement system. The design started with load pull simulation of a single HEMT cell targeting a high PAE level. The model of a unit cell transistor shows 65% maximum PAE at 10 GHz which rises up to 75% considering tuning of harmonics 2 and 3. The process uses 0.15 μ m gate length GaN 3MI on SiC from TriQuint™. The epitaxial structure used for the fabrication of the AlGaIn/GaN HEMT is grown by Metal Organic Chemical Vapor Deposition (MOCVD) on

a 3-inch semi-insulating 100 μm SiC substrate. The T-gate lengths of 150 nm are defined by electron beam lithography. The gain cut-off frequency (f_T) is beyond 80 GHz for short gate width. The nominal operating voltage is 20 V. This GaN HEMT technology presents a saturated drain current density higher than 1.15 A/mm and exhibits a peak transconductance (g_m) of 400 mS/mm. Available passives include high-voltage MIM-capacitors (>20 V) and TaN-resistors. A fully passive microstrip transmission line design-kit has been verified by measurements and implemented in ADS software.

The power amplifier topology is based on a two stage design using $10 \times 90 \mu\text{m}$ transistors. The first stage consists in 0.9 mm gate-width periphery, and the final stage is composed of four unit FET cells of 0.9 mm gate-width periphery which are 4-way combined. An electrical model of the bondwire connection at input and output pads is included in the design.

The design is focused on maximizing efficiency. This was accomplished by optimizing harmonics [9] [10], and Fig.4 details the simulated optimal impedances for 3 harmonics and resulting Γ_{load} of the output matching network for a fundamental frequency of 10 GHz.

The transistors typically have a very high gain, particularly at low frequencies which can potentially lead to stability issues. Stability series resistors have been included at the gates of the transistors and in the biasing networks as well. Additionally odd mode cancellation resistors are parts of the output combiner.

III. POWER AMPLIFIER MEASUREMENTS

In order to obtain realistic values for amplifier performance, we chose to do fixtured, as opposed to on-wafer measurement. Separated die were soldered to 40 mil thick CuMo carrier plates. The MMIC input and output bondpads were connected to 50- Ω microstrip lines on 10 mil thick alumina substrate as shown in Fig.3. Each pad is bonded with two short 1 mil diameter gold bondwires. The other end of the 50- Ω lines are connected to 2.9 mm connectorized launchers. For biasing, 0.01 μF bypass capacitors bonded to bias pads on the MMIC. The entire fixture is placed on an aluminium

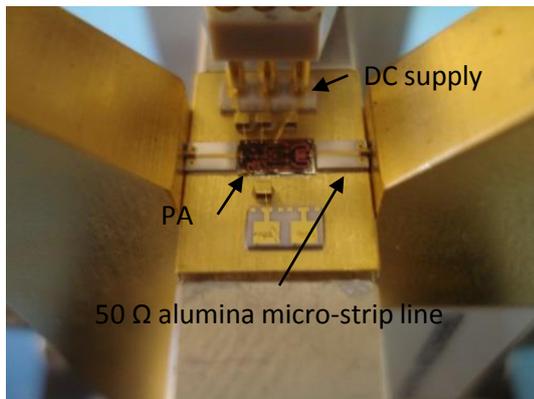


Fig. 3. Photograph of MMIC Power amplifier mounted in showing 50- Ω lines on alumina and 2.9 mm connectorized launchers as well as DC supply pins.

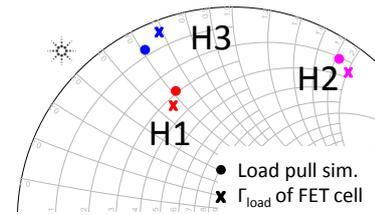


Fig. 4. Comparison of simulated optimal impedances for PAE of a $10 \times 90 \mu\text{m}$ transistor and synthesized impedances of the output matching network at 10, 20 and 30 GHz for maximum available power.

heatsink which can be fan cooled. The calibration de-embeds the measurements to the MMIC bonding reference plane. Measurement of the MMIC are then performed under continuous wave conditions at room temperature. The MMIC back side temperature was not controlled by any form of thermal management.

A. Small Signal measurement

The measured S-parameters of the circuit, using a standard VNA, are presented in Fig.5, showing a high small signal gain of 24 dB and input reflection coefficient below -9 dB from 9.7 GHz to 16 GHz at (25 V, 500 mA) bias point. Comparison with simulation proves that the model and EM simulations of passive elements predict the small signal response of the circuit. Note that the circuit design demonstrates good out of band rejection. The high gain at low frequencies may lead to stability issues.

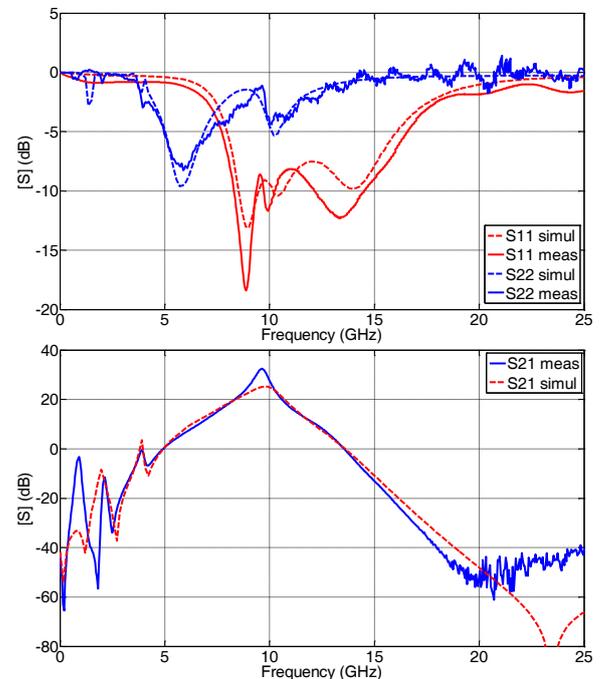


Fig. 5. Measured and simulated $|S_{11}|_{dB}$ and $|S_{22}|_{dB}$ from DC to 30 GHz (top). Measured and simulated $|S_{21}|_{dB}$ and $|S_{12}|_{dB}$ at $V_d=25$ V and $V_{g1}=-2.7$ V and $V_{g2}=-2.4$ V bias point (bottom).

B. Large Signal CW and 3rd order intermodulation measurements

The MMIC PA was also characterized using a large-signal measurement setup at ambient temperature. Fig.6 shows a power sweep performed at 10 GHz. The rising gain curve is related to the driver stage biasing point which is operating in a Class B mode.

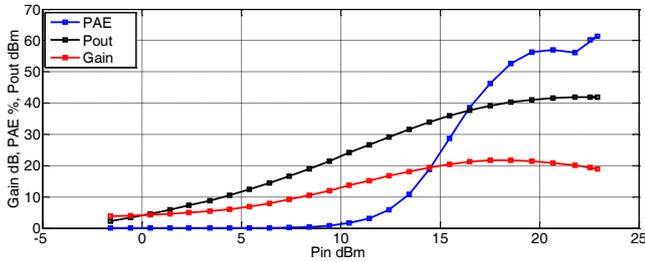


Fig. 6. Measured PAE, output power and gain at 10 GHz for $V_d=25$ V and $V_{g1}=-3.7$ V and $V_{g2}=-2.4$ V.

Additionally Fig.7 shows the resulting performance between 10 and 10.5 GHz. It is seen that the PA shows over 48% efficiency in almost the entire 500-MHz range, with a power above 10 W. The peak PAE is measured at 10 GHz to be 61% with an associated output power level of 14 W.

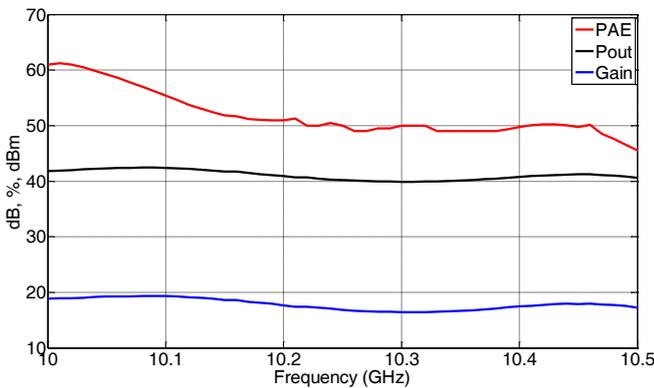


Fig. 7. Measured PAE, output power and corresponding gain over frequency for $V_d=25$ V and $V_{g1}=-3.7$ V and $V_{g2}=-2.4$ V at 22 dBm input power.

The measurement setup is based on a 4-channel time-domain receiver, operating as a large signal network analyzer (LSNA) [11]. Bi-directional couplers are implemented in the instrument to acquire absolute incident and reflected waves at the DUTs input and output ports. A relative SOLT calibration associated with a power calibration, enables accurate measurements of time-domain RF waveforms for voltages and currents at the calibration reference planes. The LSNA enables measurements in a 30 GHz RF bandwidth, and therefore only the 10-GHz fundamental and the second harmonic frequencies are measured. However, in the context of this paper, the most relevant information is at the fundamental frequency and at DC.

Time-domain voltage and current waveforms measurements at the coaxial input and output ports were acquired. All RF parameters are calculated for the voltage and current components at fundamental and DC. The large-signal input reflection coefficients are depicted in Fig.8.

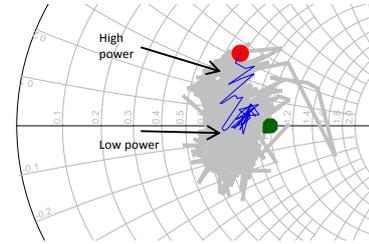


Fig. 8. Measured Γ_{in} variation as the input power swept for different bias points. Blue trace is the trajectory corresponding to the optimal gate bias voltage for PAE at 10 GHz. Grey traces are related to other bias point.

The design mainly focuses on efficiency improvement which is realized at the expense of linearity. However, most of the communication standards require the power amplifier to pass the modulation spectral mask specified at the output in order to ensure data transmission. Linearity criteria such as 2-tone testing is commonly performed as a first approach, consequently a two tone measurement has been performed with a tone spacing set to 1 MHz. The IMD3 measurement centered at 10 GHz is detailed in Fig.9. Two different biasing conditions of the driver stage have been used.

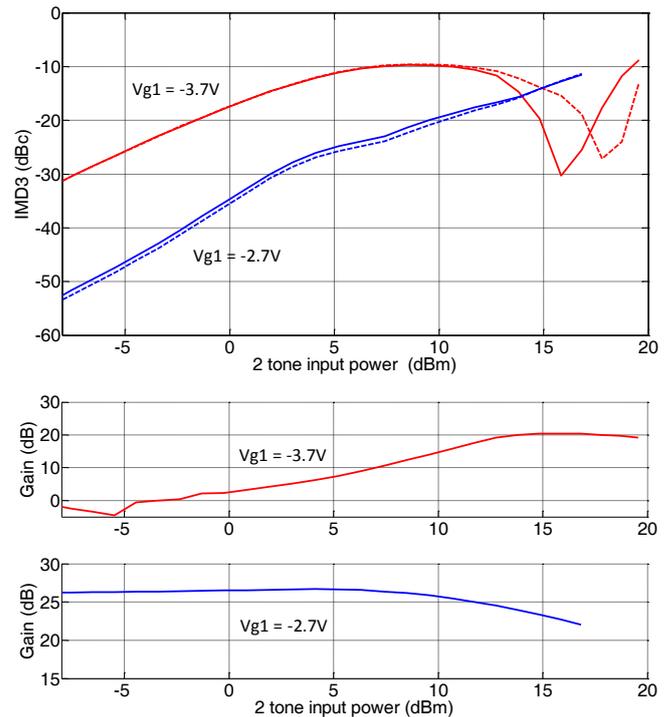


Fig. 9. Measured third order intermodulation for different classes of operation of the first stage (top). The two curves show the upper and lower sideband behavior. The corresponding gain versus total input power (bottom).

When the driver stage is biased in Class-B ($V_g=-3.7$ V) the gain curve shown in Fig.9 exhibits a strong non linearity

resulting in poor linearity performance (red curves). On the other hand when the driver stage is biased in Class-AB ($V_g = -2.7\text{V}$) the corresponding gain characteristic does not show gain expansion resulting in linearity improvement at output power back-off. At high input power levels the Class-B gain is constant over 6 dB of input power dynamic resulting in a sweet spot in IMD3 level. As a result of this behavior gate bias modulation of the driver stage would help linearity for high peak to average ratio signals.

IV. CONCLUSION

This paper discusses the design and resulting performance of a 14 W 10-GHz PA with PAE of 61%, which is among the best results obtained to date in a GaN MMIC to the best of our knowledge. The MMIC is characterized in a fixture, so the reported performance includes losses and mismatch of the bondwires and other transitions. The PAE is greater than about 50% in a 500 MHz bandwidth (10-10.5 GHz). The 4 mm \times 2.3 mm die is intended for phased array T/R modules since it is easily integrateable and does not require substantial heat-sinking.

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