Time-Domain Waveform Measurements under Large Signal RF Overdrive Stress in HEMT Technology

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I. INTRODUCTION

III-V HEMT technology is a useful choice for RF power amplifiers (PA) due to its excellent performances: high breakdown field, high output power density and high frequency operation [1]-[2]. This technology is now widely used in space equipment, which requires a thorough knowledge of its reliability and its conditions of use. Among the various tests generally carried out in a space evaluation RF step stress is an affirmed technique for the investigation of RF reliability in HEMT technology [3]-[4]. The RF step stress emulates the actual operation condition and evaluates lifetime of the transistor in a RF power amplifier. Within this work, we present in the first paragraph, an advanced time-domain methodology to investigate the device reliability and determine its Safe Operating Area. Our technique monitors in real time the RF and DC parameters in order to assess the degradation of transistors characteristics in RF power amplifiers under overdrive conditions for different load impedances. The DC parameters (V_{gs0}, V_{ds0}, I_{gs0} and I_{ds0}) and RF waveforms are continuously recorded over the time. The measured RF input and output currents and voltages at both ports of the non-linear device provide a lot of information on the degradation phenomena and are presented in the second paragraph. This technic has been tested on a GaAs PPH25X 4x36 µm pHEMT transistor from UMS foundry. This method is independent of the technology used so it is fully applicable to GaN technology. The last paragraph presents the procedure of time-domain RF stress to evaluate the reliability of GaN GH50-10 technology and the first results of characterisation protocol of RF Stress.

II. APPLICATION OF TIME DOMAIN RELIABILITY

Our set-up consists in the classic time domain load-pull set-up based on LSNA (Large Signal Network analyzer) system (Fig. 1). LSNA measures 4 periodic RF waves: the incident and reflected waves at input and output of device under test (DUT). The incident and reflected RF waves at the both port of the DUT are measured through two bidirectional couplers. These signals are then undersampled simultaneously by the four samplers of the front end of the LSNA. This undersampling principle allows the conversion and translation of the RF signal to IF bandwidth (10MHz). The resulting IF signals are digitized by 4 ADCs. Finally, a computer processes all data to get absolute phases and absolute amplitudes of fundamental and harmonic frequencies [5]. Thanks to special on-wafer absolute and relative calibration with absolute phase reference, the time domain RF voltages and currents are obtained at the DUT planes [6].

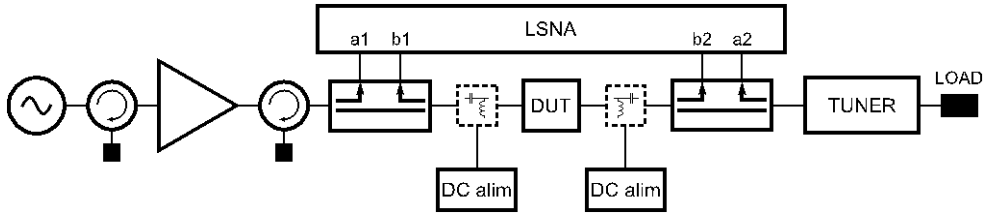

Fig. 1. Time-domain RF stress set up

RF stress under overdrive condition consists on the recording of the calibrated time domain voltage and current waveforms at both ports of the DUT driven by a CW large signal at f_0 and loaded with fixed impedances at fundamental and harmonic frequencies.

III. RESULTS OF RELIABILITY PERFORMED ON GAAS HEMT TECHNOLOGY

In this work, we compare the degradation phenomena caused by two different load impedances: the first one corresponds to a trade-off between the optimal power added efficiency and the linearity (Z_{OPT}=200Ω). The second one is chosen in order to obtain the load line slope more vertical (Z_L=50Ω): it corresponds to a high standing wave ratio (SWR) presented at the output of the transistor at the fundamental frequency. We performed RF step stresses (24 hours monitoring) with 3 different available power levels at 4 GHz corresponding to 5dBm, 10dBm and 15dBm. The device is biased in class A operation mode at a drain voltage of 6 V and a drain current of 15mA. For each RF step stress, the V_{gs0} and V_{ds0} values remain constant. During the RF stress, the DC parameters and RF waveforms were measured periodically at 5 minute intervals (monitoring). To investigate the reliability, we performed a complete "diagnosis characterization method" that consisted of full DC I-V measurements, full CW S-parameters measurements in the [2-8GHz] frequency range. Finally, full RF power sweeps were performed before and after each RF step stress. The flow chart in Fig. 2 shows the procedure of RF stress and characterization on GaAs technology.

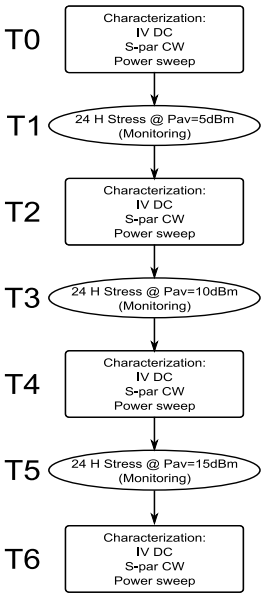

Fig. 2. Flow chart showing the procedure of characterization and time-domain RF stress on GaAs technology

The DC and RF performances are evaluated respectively through I_{gs0} and I_{ds0} recorded during the RF stress and RF figures of merit (P_{out}, gain and PAE) and RF waveforms. In Fig. 3(a), the DC evolutions are compared for two load impedances. The gate current obtained for Z_{OPT} is higher than the one measured for 50Ω because the gain compression at all fixed P_{in} is more important and the load cycle stresses the knee region (Fig. 4(d)). When Z_{OPT} is presented to the transistor, the drain current is smaller than the one consumed in mismatching impedance case (Z_L=50Ω). It can be noted in Fig. 3(b)-3(c)-3(d), that the RF figures of merit do not show any degradation over the step duration. In addition no evolution was observed between the various power sweeps performed after each step.

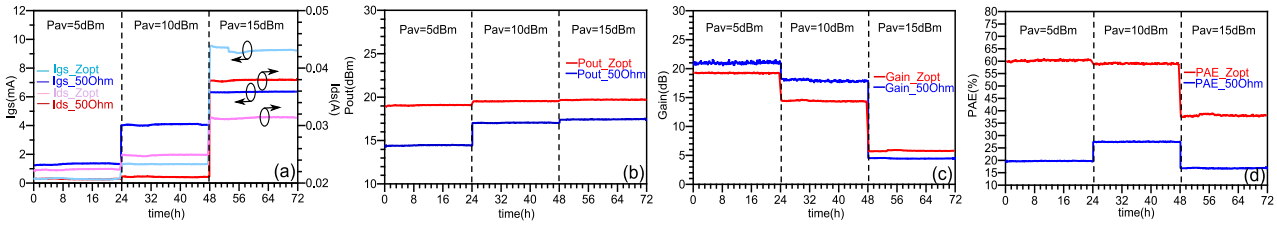

Fig. 3. (a) Comparison of DC figures of merit (at different available power) in optimum PAE and linearity impedance case and mismatching impedance case; (b) Comparison of output power (at different available power) in optimum PAE and linearity impedance case and mismatching impedance case, (c) Comparison of gain (at different available power) in optimum PAE and linearity impedance case and mismatching impedance case, (d) Comparison of power-added efficiency (at different available power) in optimum PAE and linearity impedance case and mismatching impedance case.

The periodic RF waweforms recorded, in each 24 hours step stress, are superimposed in Fig. 4.

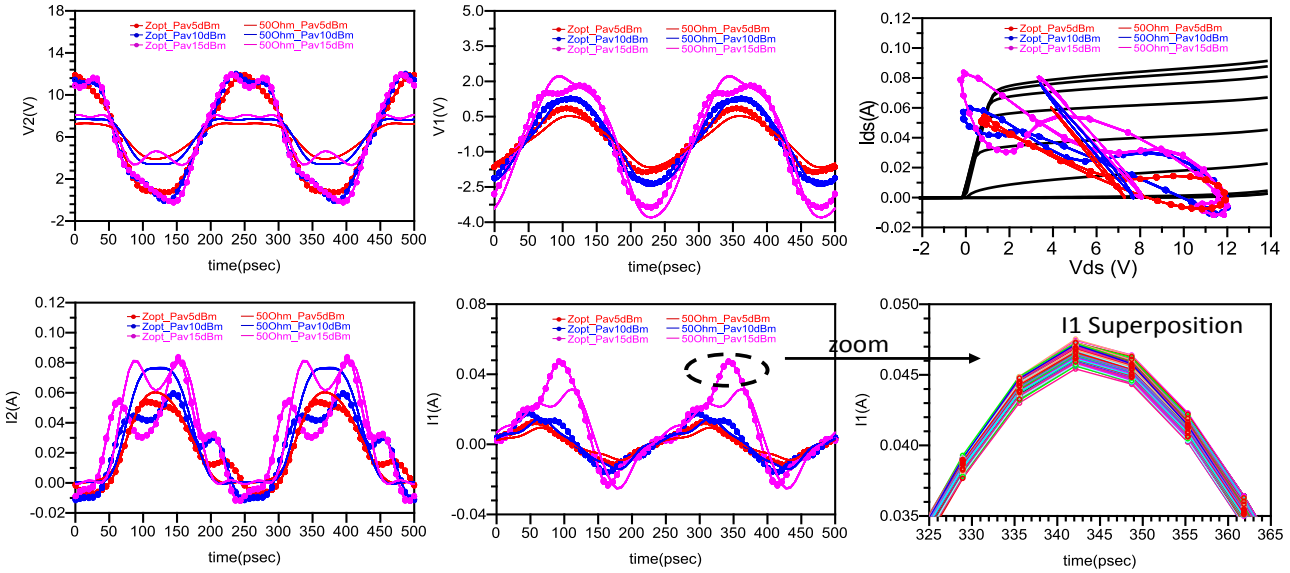

Fig. 4. (a) Comparison of V2 waveforms superposition recorded in 24 H (at different available power) in optimum PAE and linearity impedance case and mismatching impedance case; (b) Comparison of I2 waveforms superposition recorded in 24 H (at different available power) in optimum PAE and linearity impedance case and mismatching impedance case (c) Comparison of V1 waveforms superposition recorded in 24 H (at different available power) in optimum PAE and linearity impedance case and mismatching impedance case, (d) Comparison of I1 waveforms superposition recorded in 24 H (at different available power) in optimum PAE and linearity impedance case and mismatching impedance case, (e) Comparison of load cycle superposition (at different available power) in optimum PAE and linearity impedance case and mismatching impedance case, (f) Zoom of I1 waveforms superposition recorded in 24 H at Pav=15dBm in optimum PAE and linearity impedance case.

No important variation over time is observed. Obviously the time-domain waveforms with Z_{OPT} correspond to higher compression than the one measured with the mismatched impedance. According to these RF stress, the GaAs transistor do not present degradation or failure mechanism at high compression gain condition independently of the load impedance presented to the transistor.

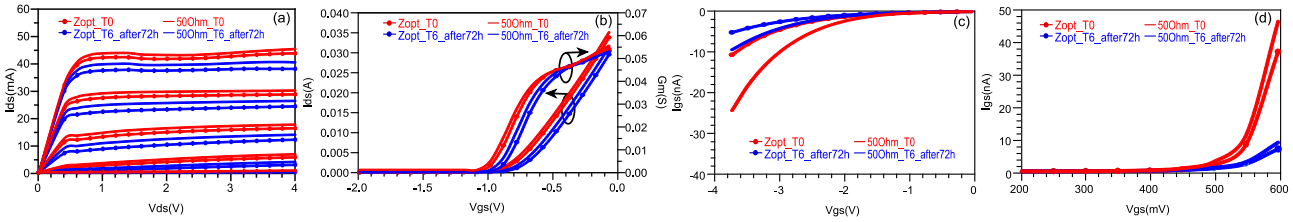

Fig. 5. (a) Comparison of DC I-V characteristic (Vgs from -0.96V to 0V – step -0.24V) before and after 72h of stress at optimum PAE and linearity impedance case and mismatching impedance case; (b) Comparison of gm and Ids versus Vgs (measured at Vds=4V) before and after 72h of stress at optimum PAE and linearity impedance case and mismatching impedance case; (c) Comparison of gate current versus gate tension (Vgs from -4V to 0V) before and after 72h of stress at optimum PAE and linearity impedance case and mismatching impedance case; (d) Comparison of gate current versus gate tension (Vgs from 0.2V to 0.6V) before and after 72h of stress at optimum PAE and linearity impedance case and mismatching impedance case.

The DC measurements presented in Fig. 5 show constant variations of transistor characteristics after 72 hours of RF stress for both load impedances. (T2 and T4 characteristics are not reported). A decreased gate current was recorded with an increased RF power stress level, in particular for optimum PAE and linearity impedance case. This phenomenon is due to higher gain compression applied to transistor. The change of the Ig-Vg characteristic produces the variation of the S11-parameter amplitude, as shown in Fig. 6(a). CW S-parameters measurements are presented in Fig. 6. It can be noted that only small variation of S-parameter between 2-8 GHz occurred after a 72 H RF stress (T6) whatever load impedance is. It means that even if a small degradation of gate current is observed for GaAs HEMT technology, the RF small signal characteristics are not affected by the RF stress of the transistor. This conclusion is a first step for the space qualification of this technology. Fig 7 shows the comparison of large signal performances of the component before and after stress protocol.

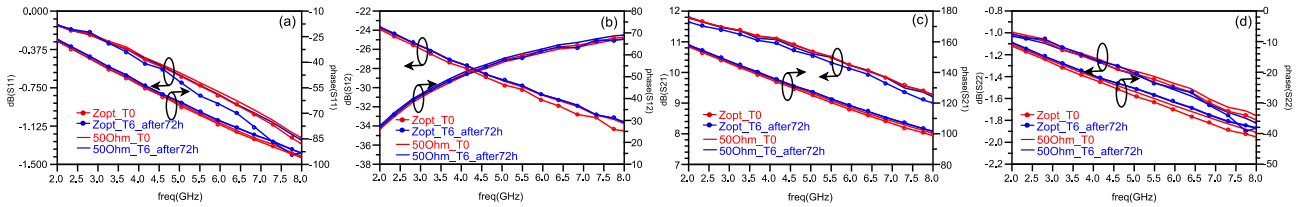

Fig. 6. (a) Comparison of S11 (freq from 2GHz to 8GHz) before and after 72h of stress at optimum PAE and linearity impedance case and mismatching impedance case; (b) Comparison of S12 (freq from 2GHz to 8GHz) before and after 72h of stress at optimum PAE and linearity impedance case and mismatching impedance case; (c) Comparison of S21 (freq from 2GHz to 8GHz) before and after 72h of stress at optimum PAE and linearity impedance case and mismatching impedance case; (d) Comparison of S22 (freq from 2GHz to 8GHz) before and after 72h of stress at optimum PAE and linearity impedance case and mismatching impedance case.

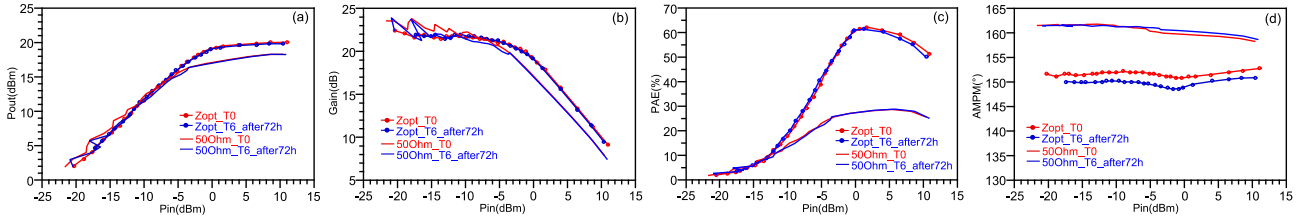

Fig. 7. (a) Comparison of output power versus input power before and after 72h of stress at optimum PAE and linearity impedance case and mismatching impedance case; (b) Comparison of gain versus input power before and after 72h of stress at optimum PAE and linearity impedance case and mismatching impedance case; (c) Comparison of PAE versus input power before and after 72h of stress at optimum PAE and linearity impedance case and mismatching impedance case; (d) Comparison of AMPM versus input power before and after 72h of stress at optimum PAE and linearity impedance case and mismatching impedance case.

It can be also concluded that no significant variation of large signal performances are induced by the RF stress protocol. As the overall performances remain constant during the application of the stress protocol the GaAs technology appears as a good candidate for space qualification.

The good capability of the time domain RF stress is demonstrated on stable GaAs technology, so now the same method is used to test the reliability of wide band-gap technologies as GaN transistor.

IV. PROCEDURE OF TIME-DOMAIN RF STRESS ON GAN HEMT TECHNOLOGY

The same set-up is used and, in the “characterization protocol”, other measurements (pulsed IV measurements) are introduced to have more information on trapping states of GaN transistor. Pulsed S-parameters measurements combined with pulsed IV measurements and power sweep measurement allow the extraction of the electrothermal model during the RF step stress [7]. The procedure of RF stress and new characterization on GaN technology is shown in the flow chart (Fig. 8).

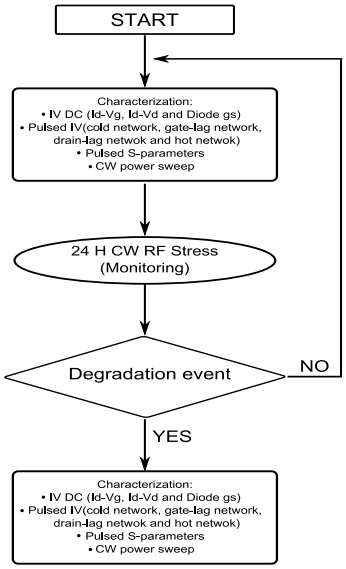

Fig. 8. Flow chart showing the procedure of new characterization and time-domain RF stress on GaN technology.

For this study, we used GH50-10 8x250µm GaN transistor. We performed RF step stresses with a 24 hours monitoring for different values of gain compression at 4GHz. The device is biased in class AB operation mode (50mA of drain current at 50V of drain voltage). The load impedance, presented during the RF stress, is chosen to have the optimal power added efficiency.

In order to obtain the information trapping phenomena, 4 pulsed I-V measurements from different quiescent points (with short pulses 1µs to have a quasi-isolation measurement) are performed:

- Cold network: the quiescent point is V_{gs0}=0V and V_{ds0}=0V to avoid trapping events;
- Gate-lag network: the quiescent point is V_{gs0}=-2.4V (pinched off) and V_{ds0}=0V to analyse the trapping phenomena caused by off-state condition imposed to gate voltage.
- Drain-lag network: the quiescent point is V_{gs0}=-2.4V (pinched off) and V_{ds0}=50V to analyse the trapping phenomena caused by combination between off-state condition (imposed to gate voltage) and high drain voltage.
- Hot network: the quiescent point is V_{gs0}=-2.04V and V_{ds0}=50V (Ids=50mA) to analyse the trapping phenomena caused by class AB operation mode.

The results of pulsed I-V measurements are shown in Fig. 9 (a). No gate-lag trapping phenomena are noticed. However, strong drain-lag phenomena can be observed (e.g. 22% less between cold network and drain-lag network at Vds=20V). More important current collapse is observed in hot network.

In Fig. 9 (b) the RF large signal characteristics obtained from load pull measurements are presented. They are obtained for load impedance Z_{L_OPT}=19.12+j52.75 Ω corresponding to the optimal PAE operating mode of the transistor at 4 GHz.

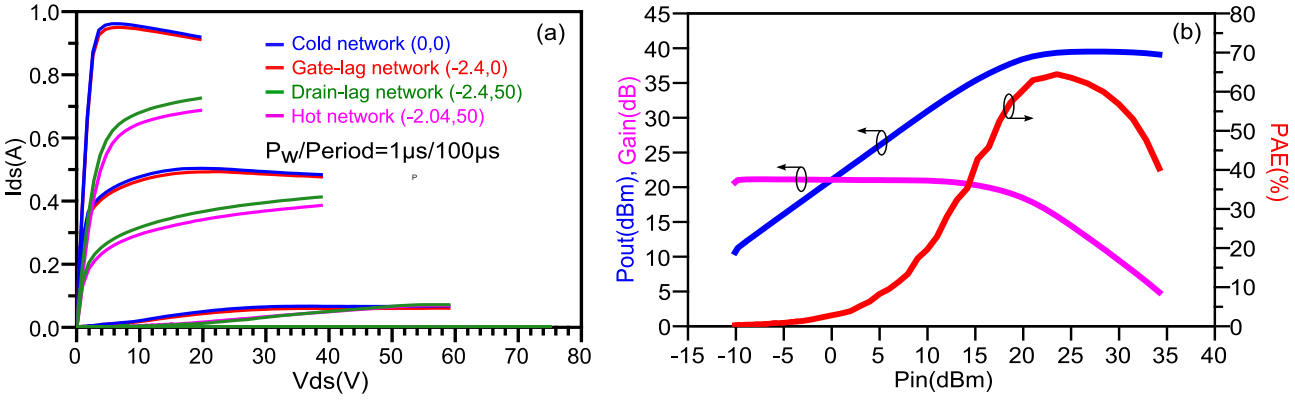

Fig. 9. (a) Comparison of pulsed I-V measurements from different baselines. The gate terminal is pulsed from 0V to -3V with 1V of step (b) RF power sweep at 4GHz (Z_{L_OPT}=19.12+j52.75 Ω).

The pulsed S-parameters are extracted for different biasing points in the ideal load line (from 0.5GHz to 20 GHz) of the large signal operating mode (quiescent point : V_{ds0}=50V and I_{ds0}=50mA) are shown in Fig.10.

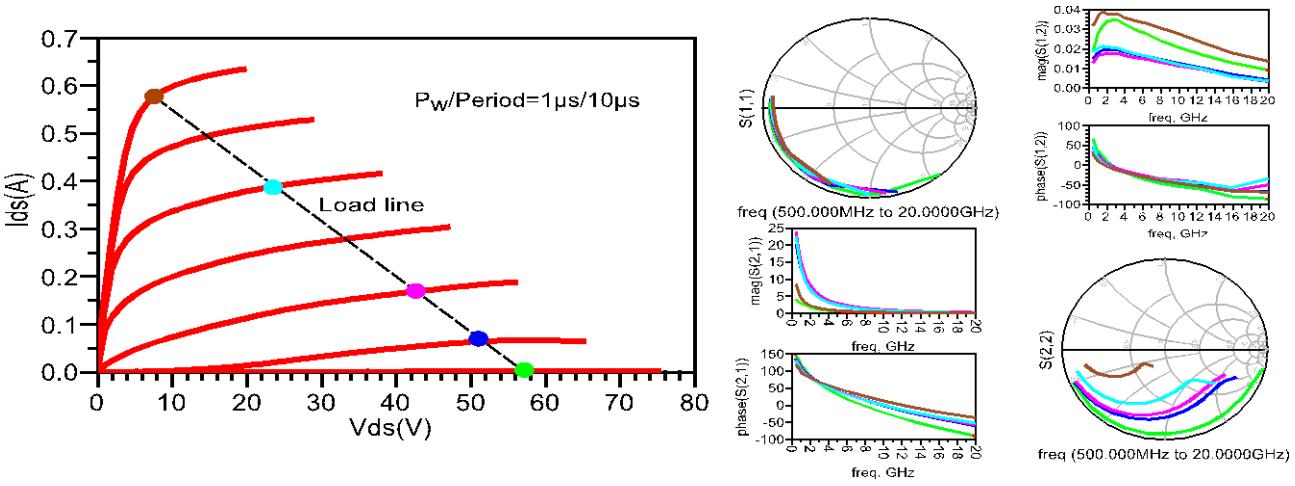

Fig. 10. Pulsed S-parameters extract to load line at quiescent point V_{gs0}=-2.04V and V_{ds0}=50V.

The main objective of the future work consists in extracting this electrothermal model at different steps of the step stress to evaluate the evolution of values of the different model parameters.

V. CONCLUSION

In this work, we discussed an advanced time-domain methodology to investigate the reliability and determine the Safe Operating Area of HEMT transistors. The main of objectives of this procedure is to help the MMIC designer to improve the quality of space equipment, taking to account overdrive performances of transistor and the associated large-signal electrical model. This procedure has been successfully applied on GaAs HEMT technology. The results confirm that the GaAs HEMT has a good robustness and reliability and they validate the UMS pHEMT technology for space applications.

GaN HEMT technology is now under testing with same time-domain methodology and first results of characterization protocol have been presented. The GaN reliability results will be presented during the workshop session.

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