WSM: Characterization of transistor drain supply terminal impedance at signal envelope frequencies

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WMC: The Importance of Low-frequency Measurements on High-frequency Characterization
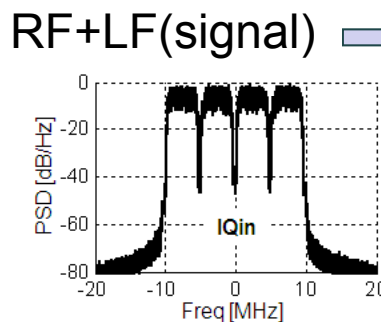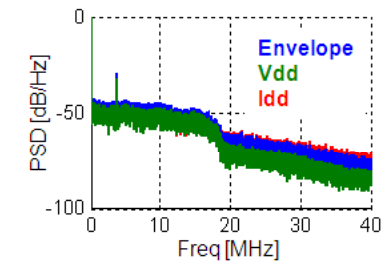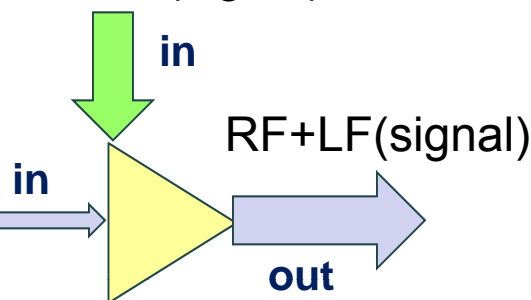
Outline and Topics

➢ Some applications that require low-frequency characterization of microwave components or devices

➢ Supply modulated PAs and drain supply characterization

➢ "Time reversal" of PAs – transistor rectifier characterization

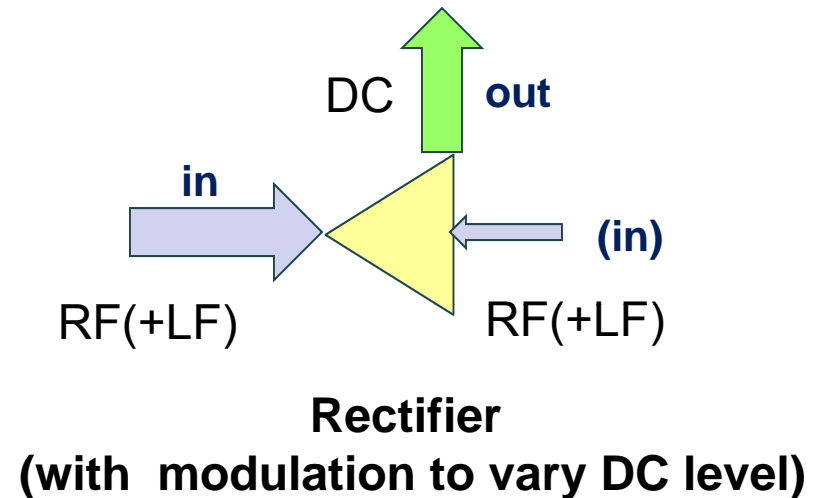➢ What has not been done but would be useful

Bias and signals

DC+LF(signal)

in

RF+LF(signal)

in

RF+LF(signal)

out

**Amplifier with
Supply Modulation**

DC   **out**

in

(in)

RF(+LF)   RF(+LF)

**Rectifier
(with modulation to vary DC level)**

- ➤ Applications:
  - ➤ Efficient power amplifications of increasingly difficult signals
  - ➤ Wireless powering, power beaming, fast dc-dc conversion
- ➤ Supply dynamically modulated at signal (LF) bandwidth to improve PA efficiency – requires modeling at very different time scales
- ➤ Modulating a RF powering signal allows for improved conversion efficiency or variable DC power level
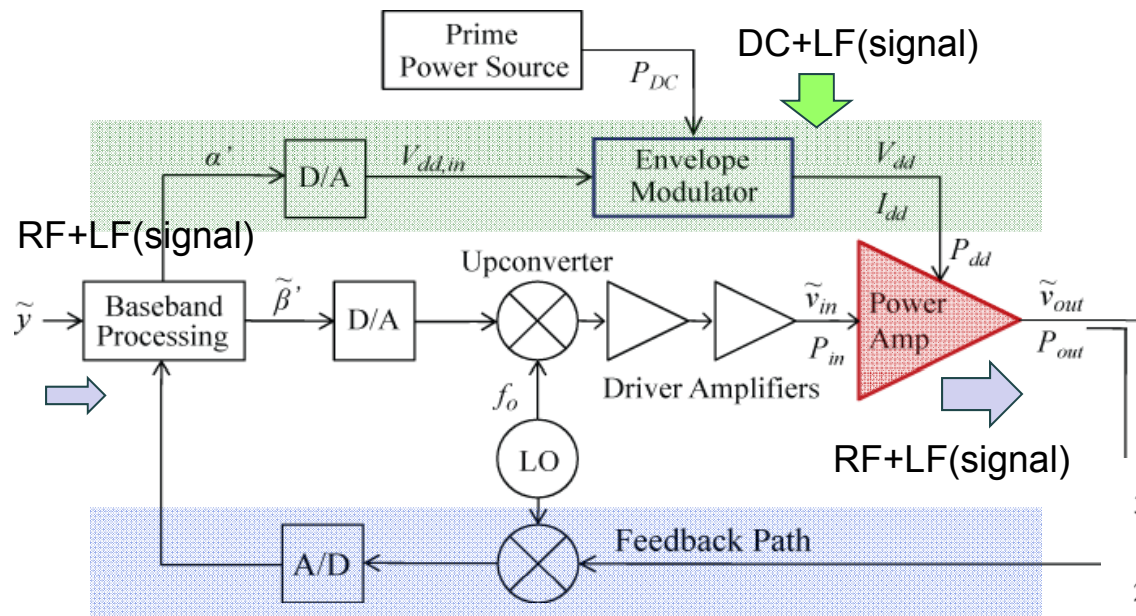
Motivation:
high efficiency for high PAR signals

- PA consumes most power
  - 1.4W required for cooling, power distribution, etc, for each 1W dissipated

- **Traditional high-PAR PA efficiency**
  - Efficiency degrades with reduced output power
  - Average efficiency is low for high-PAR signals

- **Techniques in this work**
  - Raise PA efficiency at PEP with harmonic-tuned PA design to >80%
  - Extend high-efficiency PA operation to average power level

	30% Efficiency	50% Efficiency
RF Output Power	50W	50W
Dissipated in PA	117W	50W
Dissipated by cooling, distribution, etc.	165W	71W
Total Input Power	332W	171W
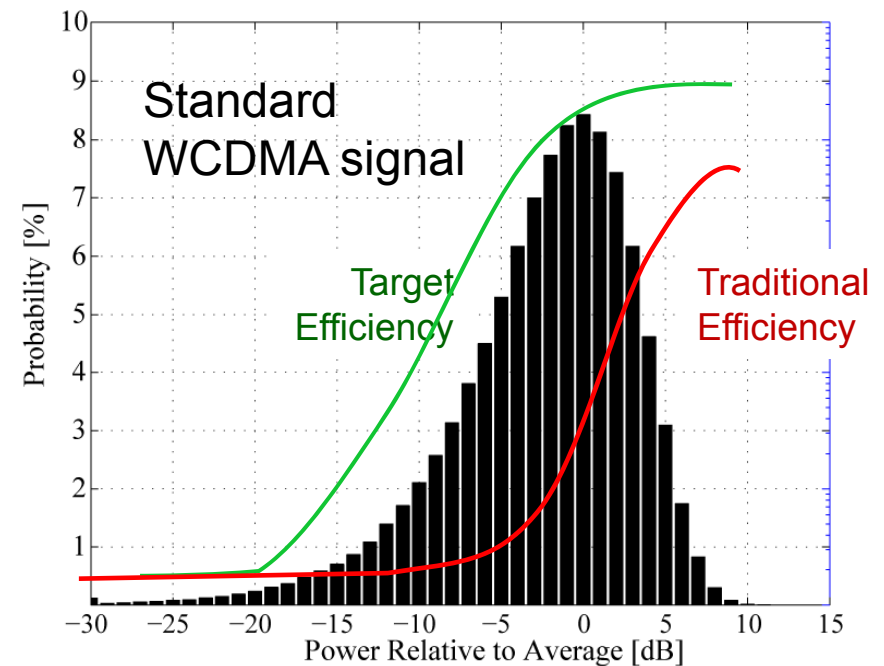
Supply-modulated PAs

- Most of the envelope modulates the supply
- A portion of the envelope modulates the drive
- The trajectory optimizes efficiency
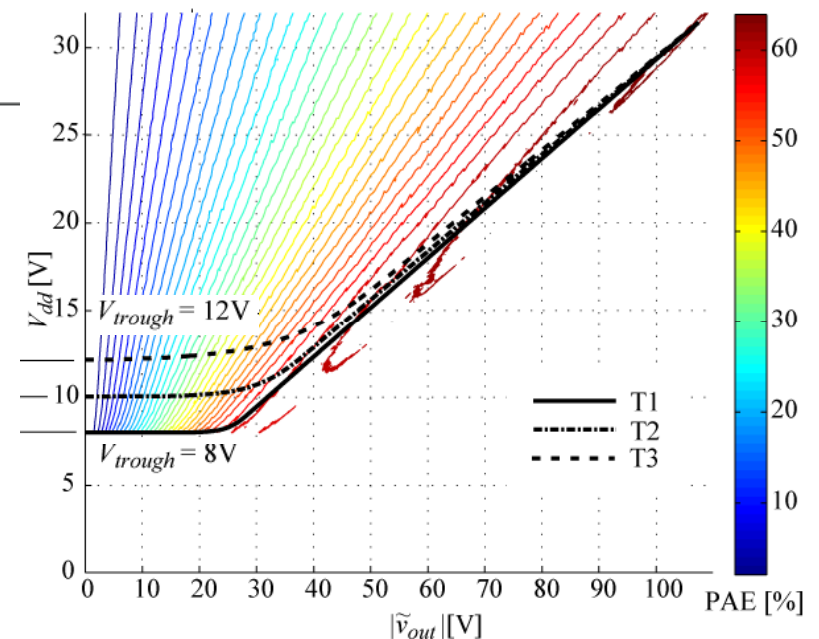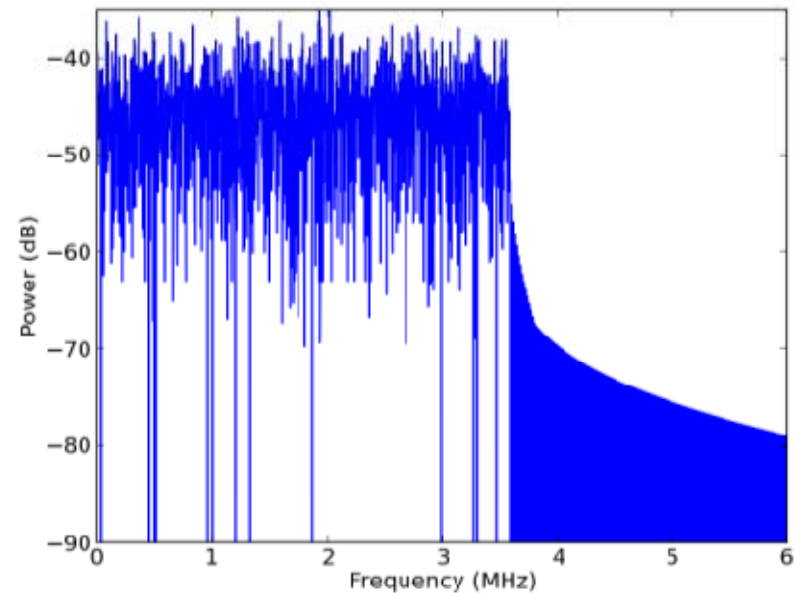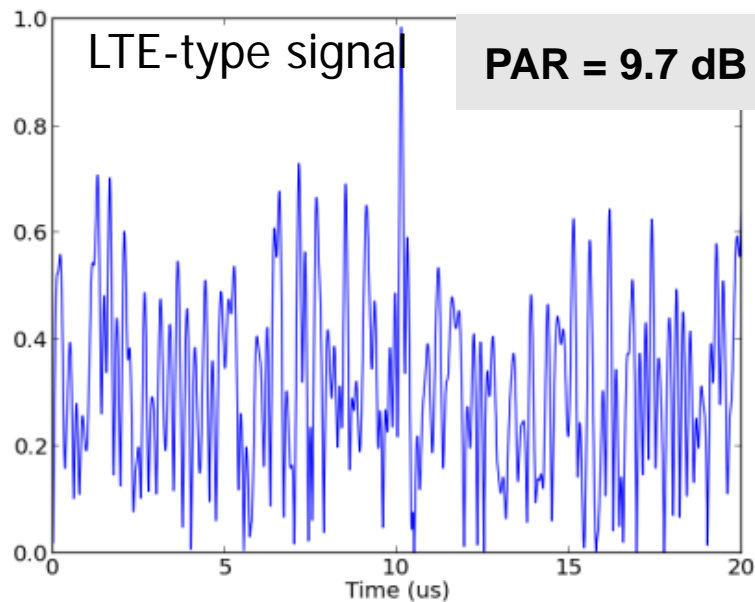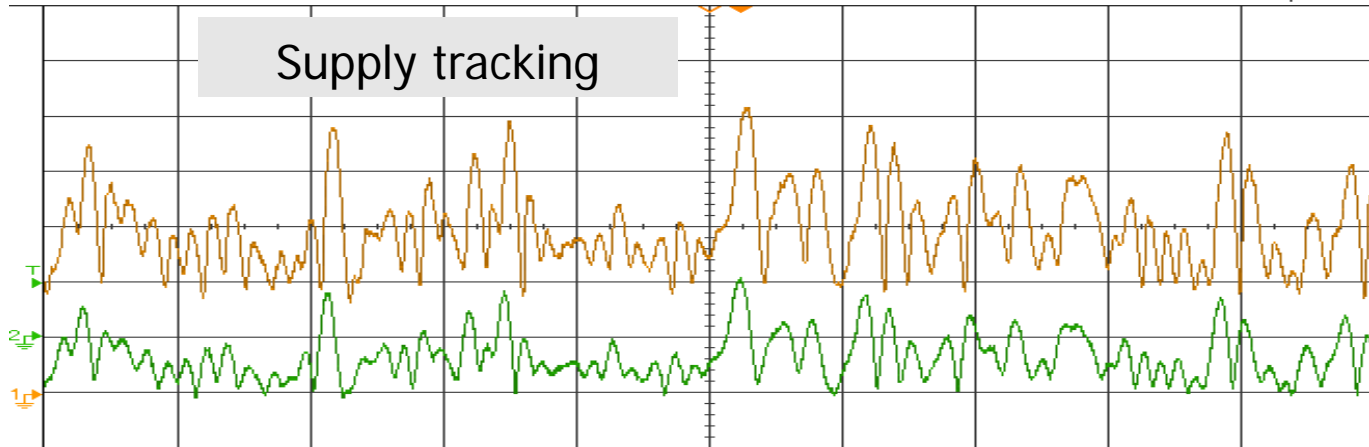
- Measured GaN PA at 2.14GHz
- Three example trajectories perform tradeoff between PA efficiency and supply modulator requirements

Example low-bandwidth high PAR signal

LTE-type signal   **PAR = 9.7 dB**

Supply tracking

Result with high efficiency supply modulator

Input pdf

Output pdf, Vdd constant

Vdd = 28V,
PAE=36.9%

Vdd = 30V,
PAE=39.5%

Output pdf, dynamic Vdd

Integrated
S-band PA with DSM1
PAE~50%
CPAE 40-45%

*PAE ~ 56% for higher
input powers

Supply Modulated
Input
Vdd = 30 V
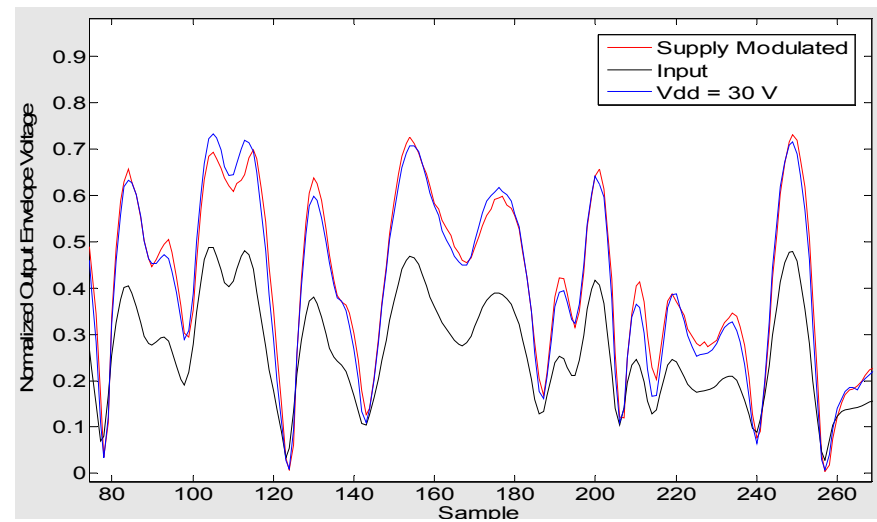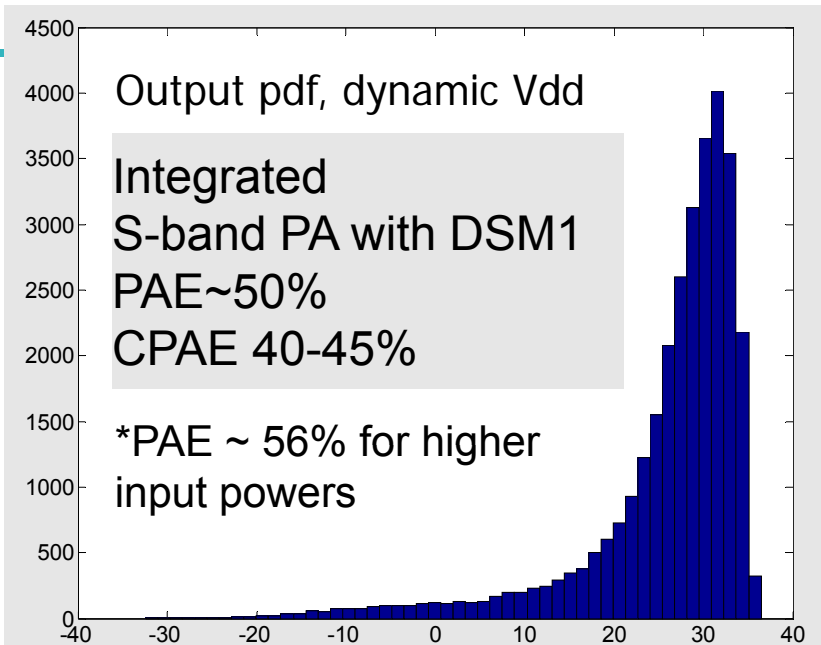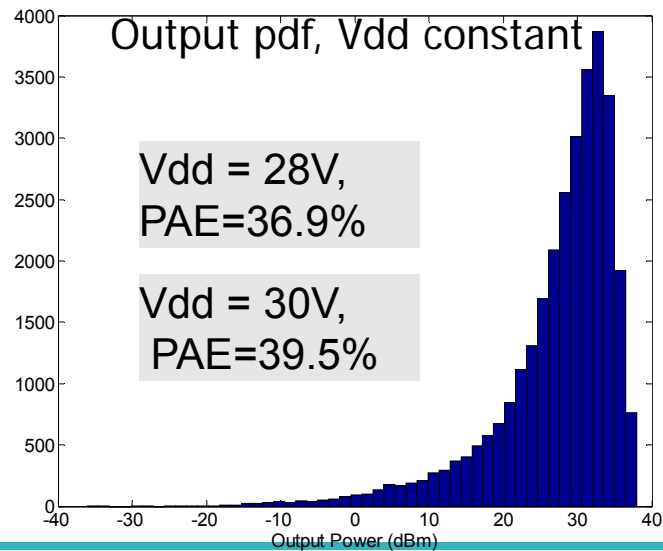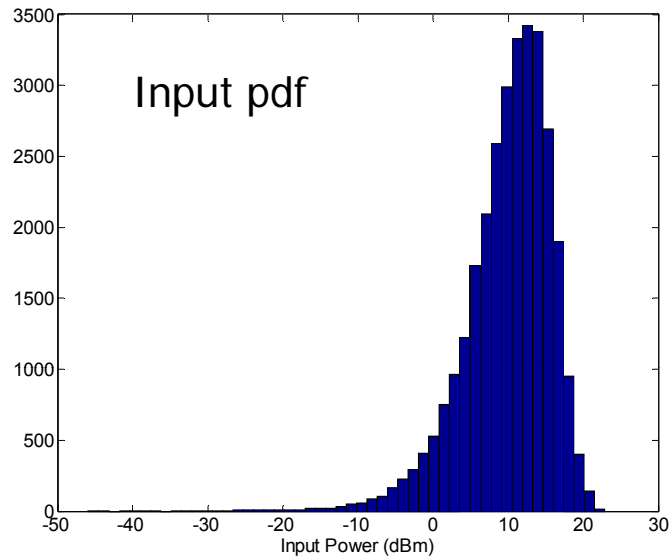
Increased bandwidth high PAR signal

OFDM signal

PAR = 9.1 dB
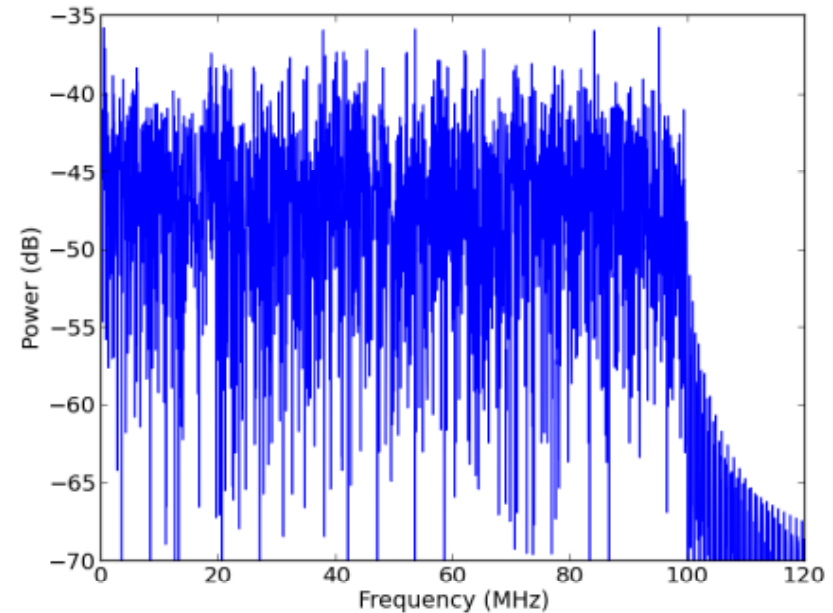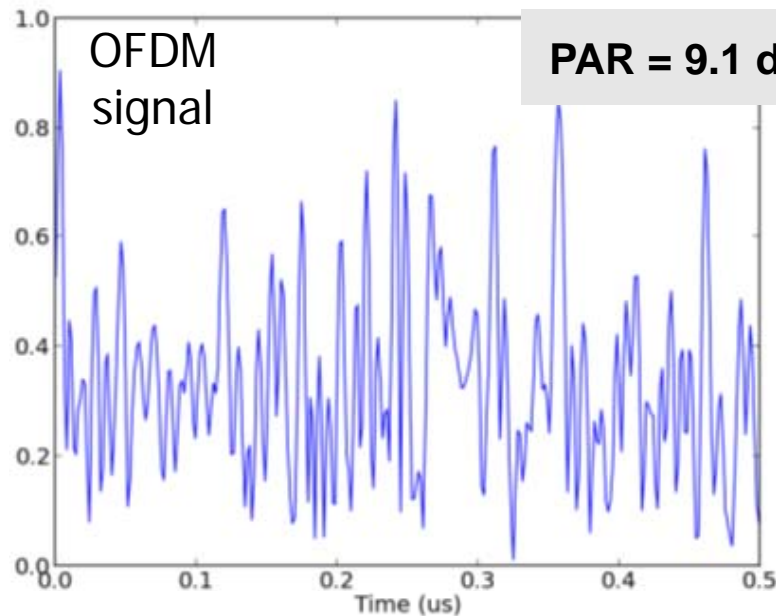
DSO-X 3034A, MY51351637: Fri Oct 26 14:36:06 2012

Supply tracking
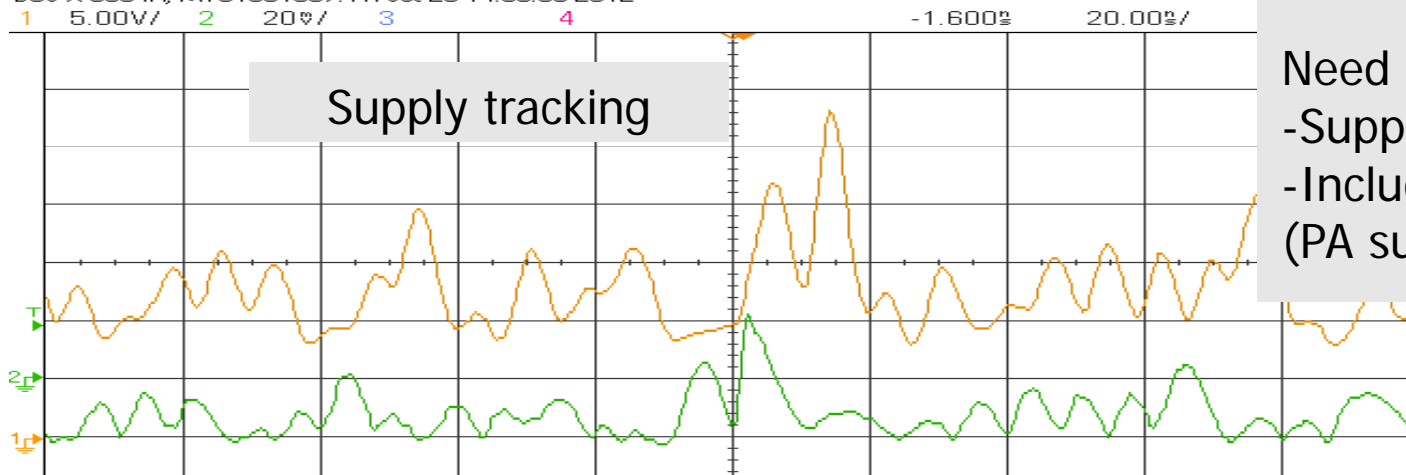
Need better:
- Supply design
- Includes knowing load (PA supply terminal)

Dynamic resistance

- Trajectory T1 clearly has amore dynamic drain impedance than T3
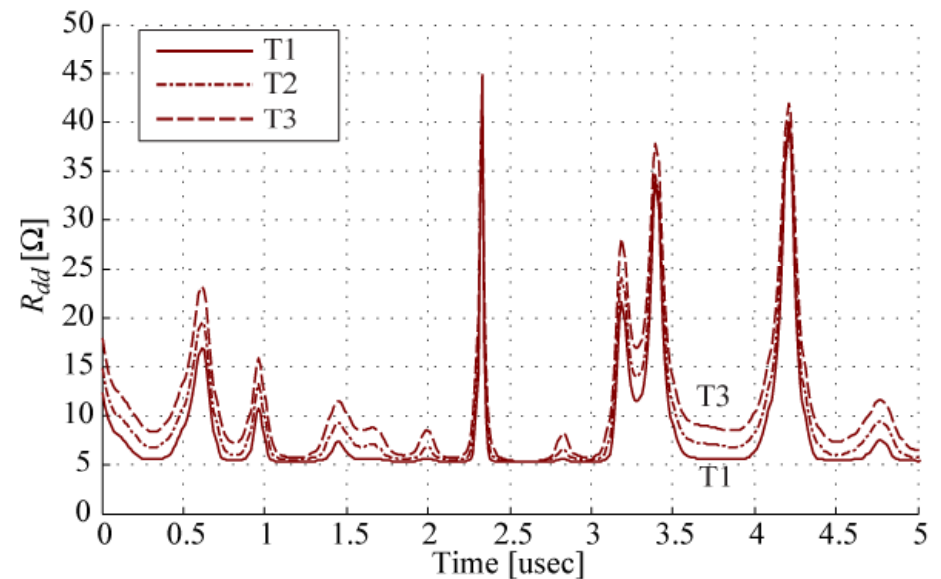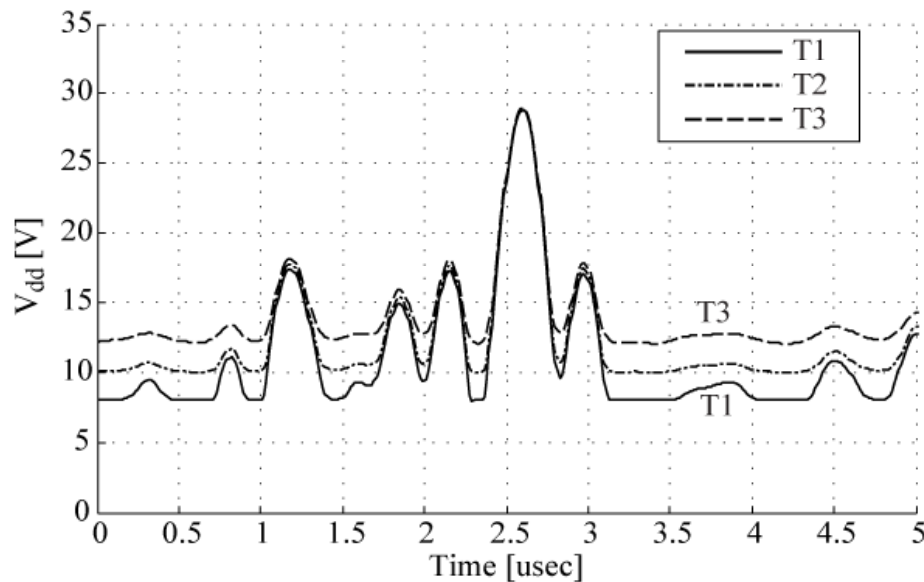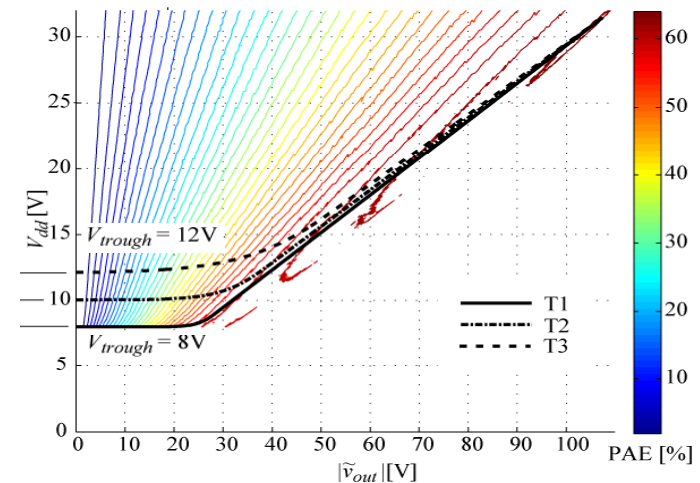- Can we quantify and how does it impact PA design?

$$R_{dd} = \frac{V_{dd}^2 \eta_d}{P_{out}}$$

Simulated drain resistance
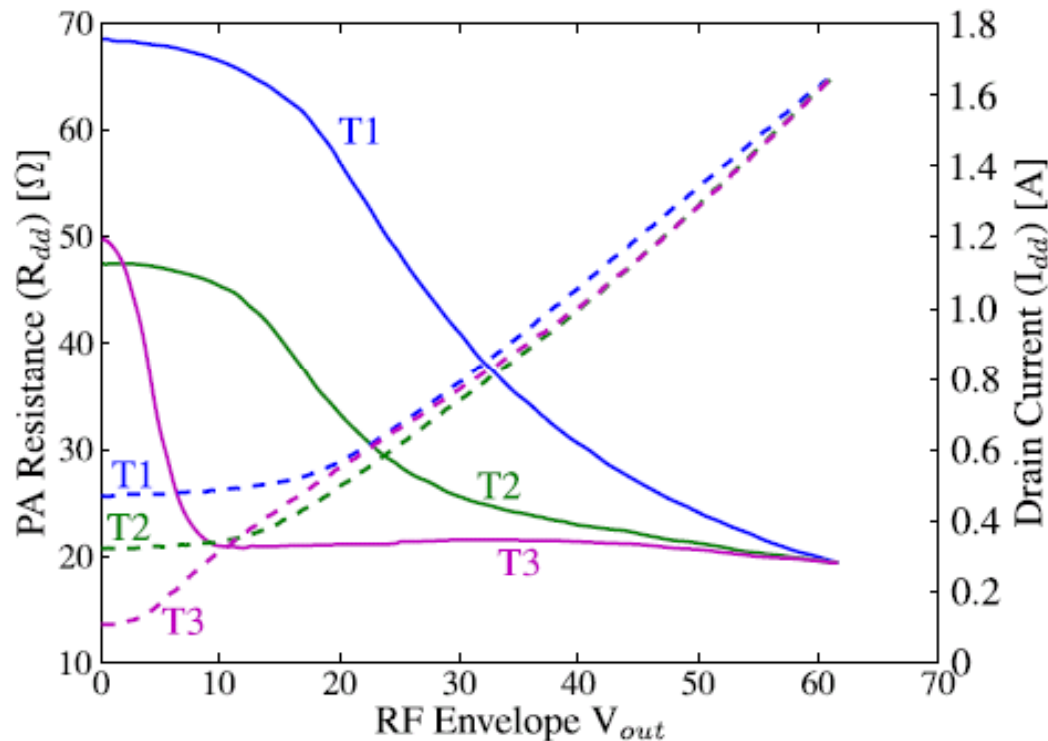
$$R_{dd} = V_{supply} / I_{supply}$$

$$R_{dd} = V_{supply}^2 \cdot \eta_d / P_{out}$$

At higher bandwidth, cannot be assumed to be purely real

- R_{dd} not directly related to PA load line; made constant over RF cycle by RFC
- the output impedance of the SM should be kept low over a wide frequency range to limit V_{supply} error due to voltage division between the supply modulator output impedance and load PA impedance
- R_{dd} and I_{dd} both vary a lot more for T3 than for T2

PA dynamic impedance measurement

- Bias tee is no longer a DC path

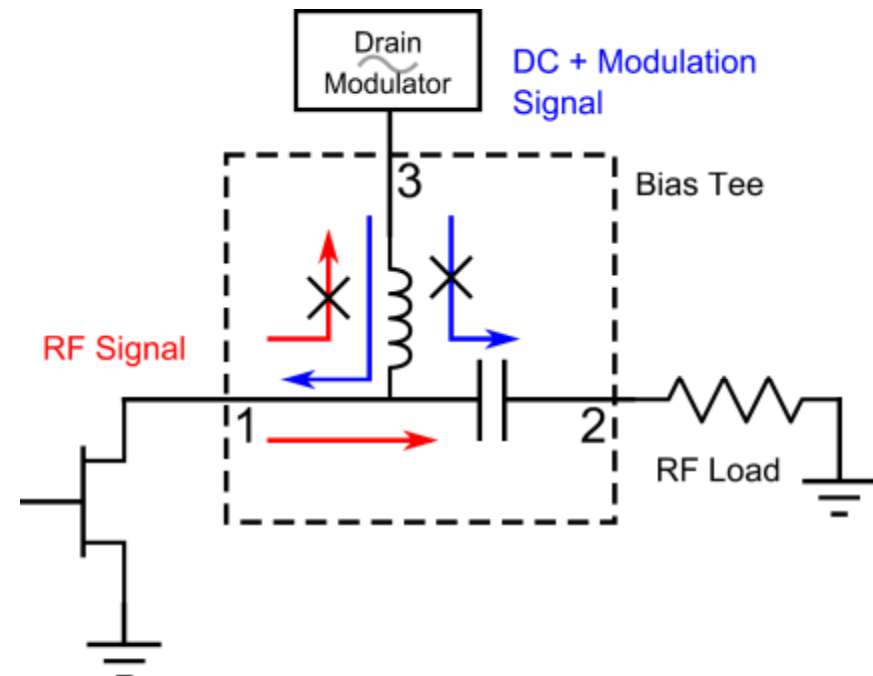- Can the bias tee and output of the PA be optimized for drain modulation?

- Purpose of the drain bias tee is to direct the modulation signal to the transistor

- Desired bias tee S-parameters:

$$S(f_{BB}, f_{RF}) = \begin{bmatrix} 0,0 & 0,1 & 1,0 \\ 0,1 & 1,0 & 0,0 \\ 1,0 & 0,0 & 0,1 \end{bmatrix}$$
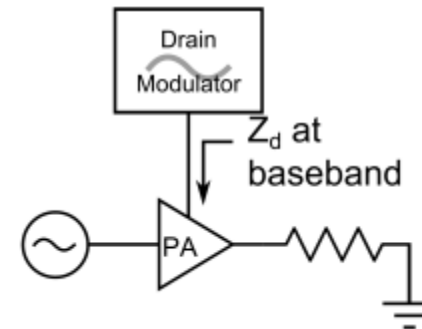
Complex drain impedance measurement
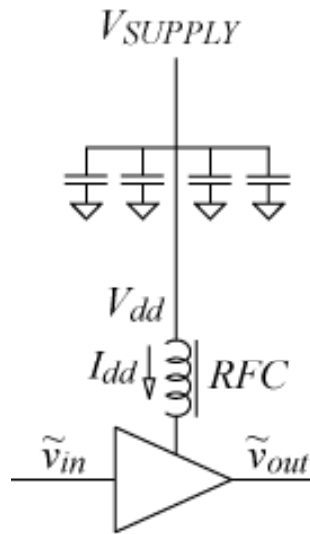
Traditional bias network
- Bypass caps
- Source large dynamic currents
- Reject ripple at high frequency

SMPA bias network
- EM+interconnect
- Low **large-signal** output impedance required over **wide frequency** range

- Determine complex impedance by voltage waveforms with oscilloscope (V_1, V_2)

- Calibration allows measurement plane to be moved to transistor

Calibration for drain impedance measurement
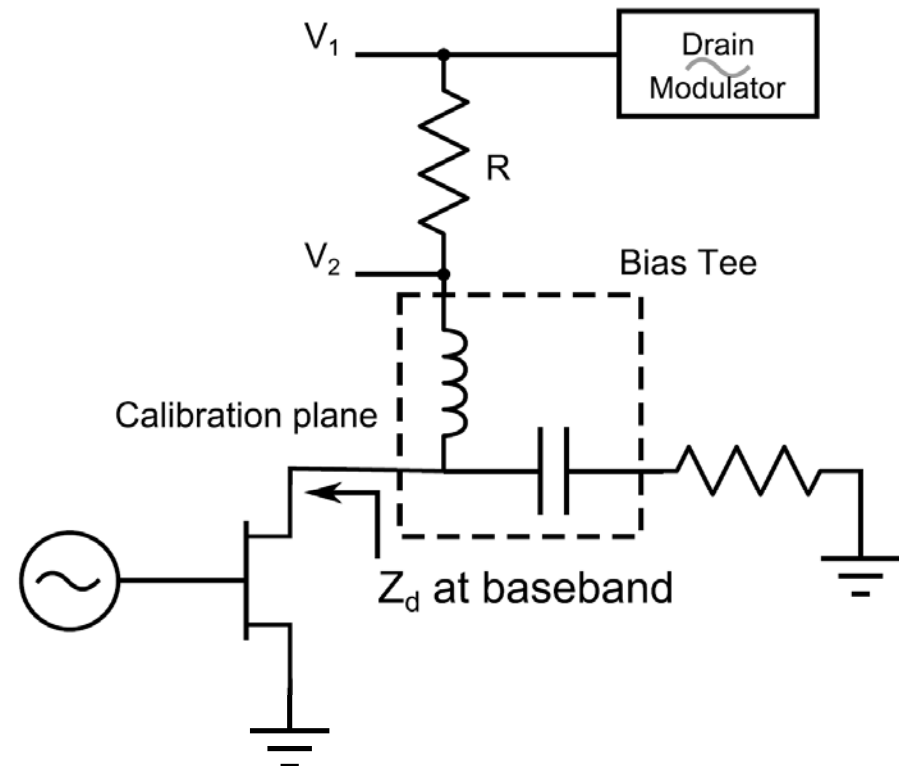
- A reflection coefficient ($M_{A,B,C}$) can be found from the two complex voltages V_1, V_2

- Use 3 known standards A_{11}, B_{11}, C_{11}
  - Similar to Short-Open-Load calibration

- Can find S-parameters of Error Box [L]:

$$\begin{bmatrix} 1 & A_{11}M_A & -A_{11} \\ 1 & B_{11}M_B & -B_{11} \\ 1 & C_{11}M_C & -C_{11} \end{bmatrix} \begin{bmatrix} L_{11} \\ L_{22} \\ \Delta L \end{bmatrix} = \begin{bmatrix} M_A \\ M_B \\ M_C \end{bmatrix}$$
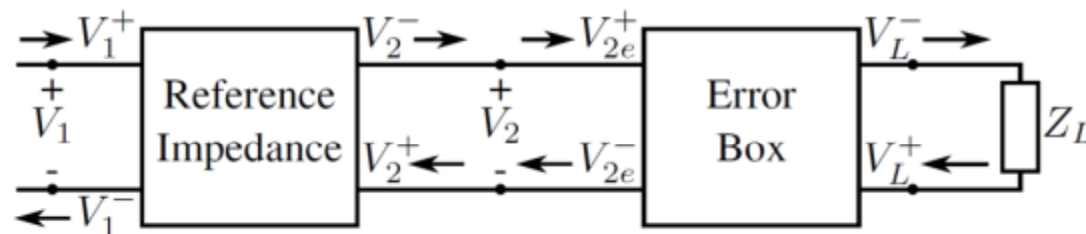
Design of a LF/RF bias Tee

- Simulated Bias Tee
  - RF-Low Frequency Isolation > 30 dB
  - 0.8 GHz RF match (-20 dB)
  - Low frequency and RF through loss < 0.25 dB
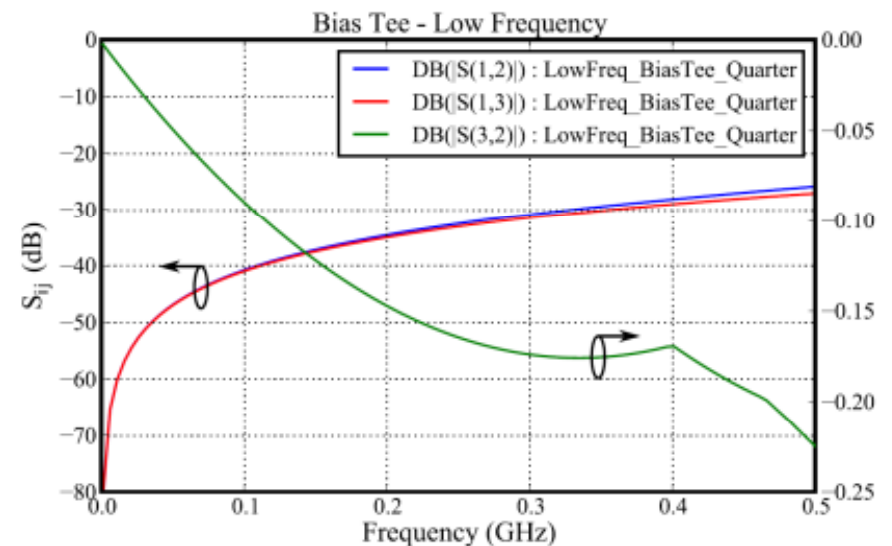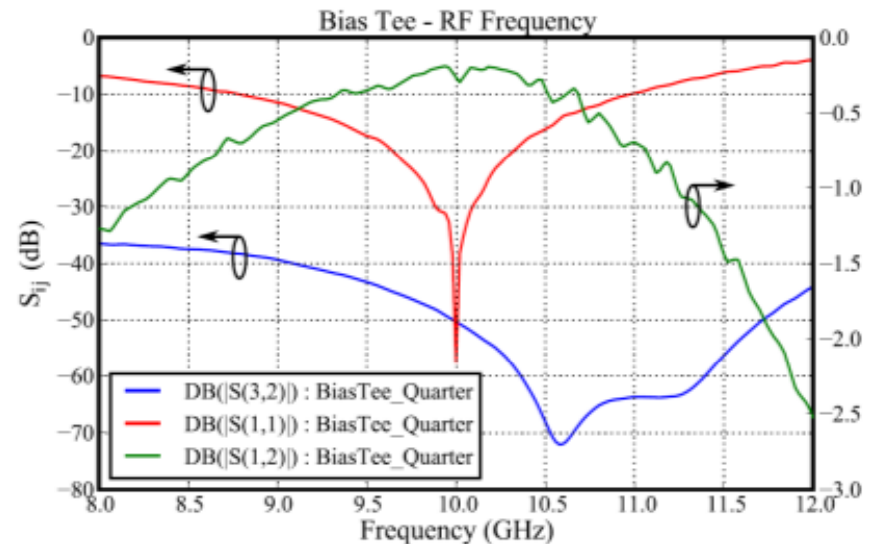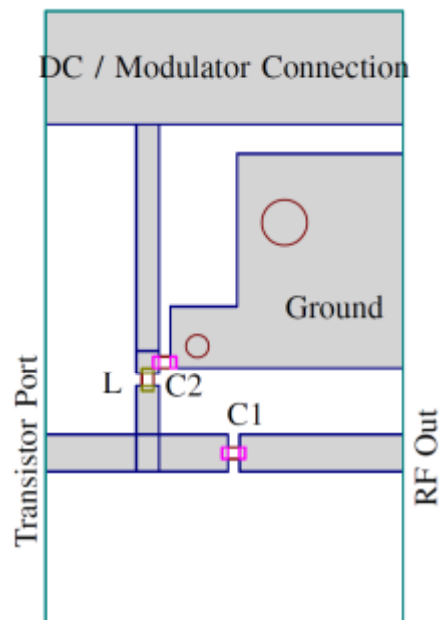
Drain impedance: calibration validation

- To verify the calibration and setup, a few arbitrary lumped impedances were measured

- Measuring waveforms with low amplitudes is difficult (short, open)

- Accuracy of $Z_L \pm 5\%$

Reference Impedance (101 + 82pF)

Legend:
- Re[Z_{ideal}]
- Im[Z_{ideal}]
- Re[Z_L] ($Z_r = 10\Omega$)
- Im[Z_L] ($Z_r = 10\Omega$)
- Re[Z_L] ($Z_r = 33\Omega$)
- Im[Z_L] ($Z_r = 33\Omega$)
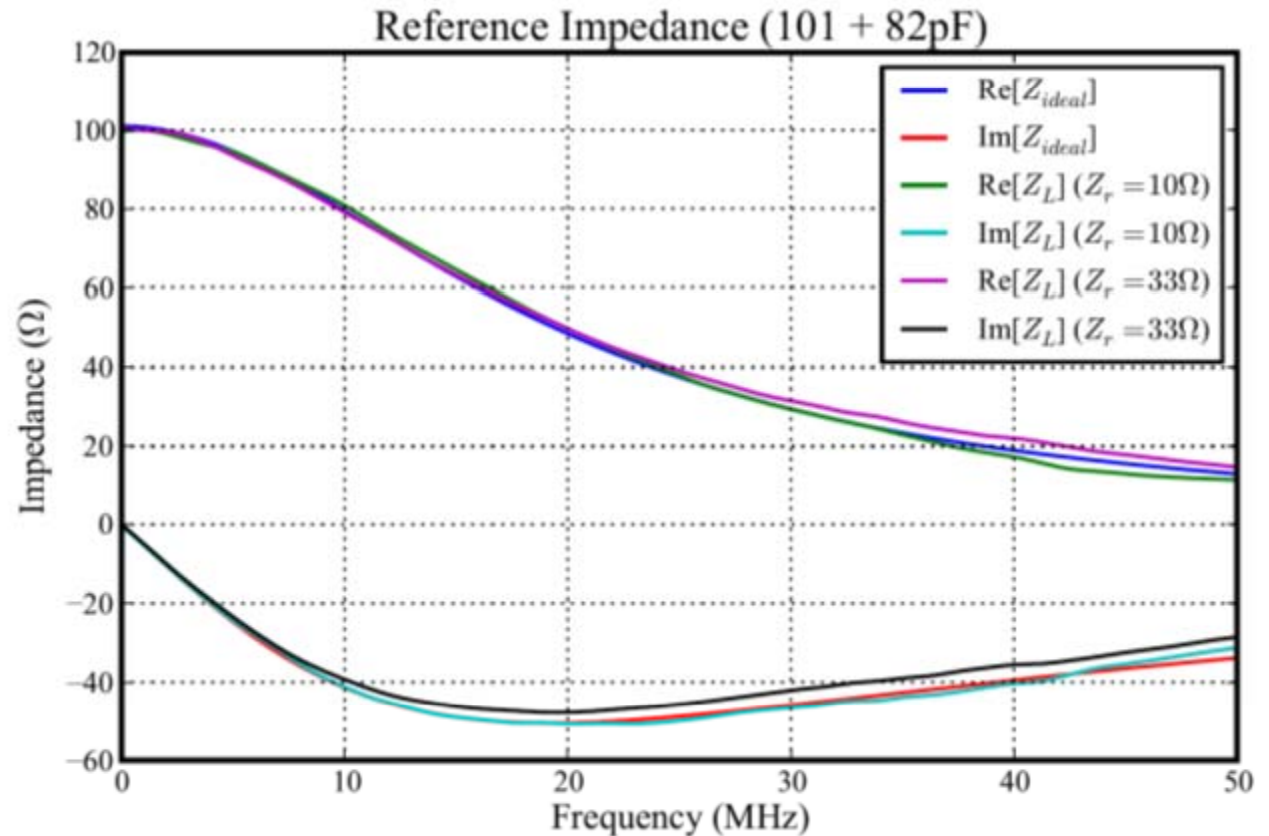
Drain impedance measurements: transistor vs. PA, no RF drive
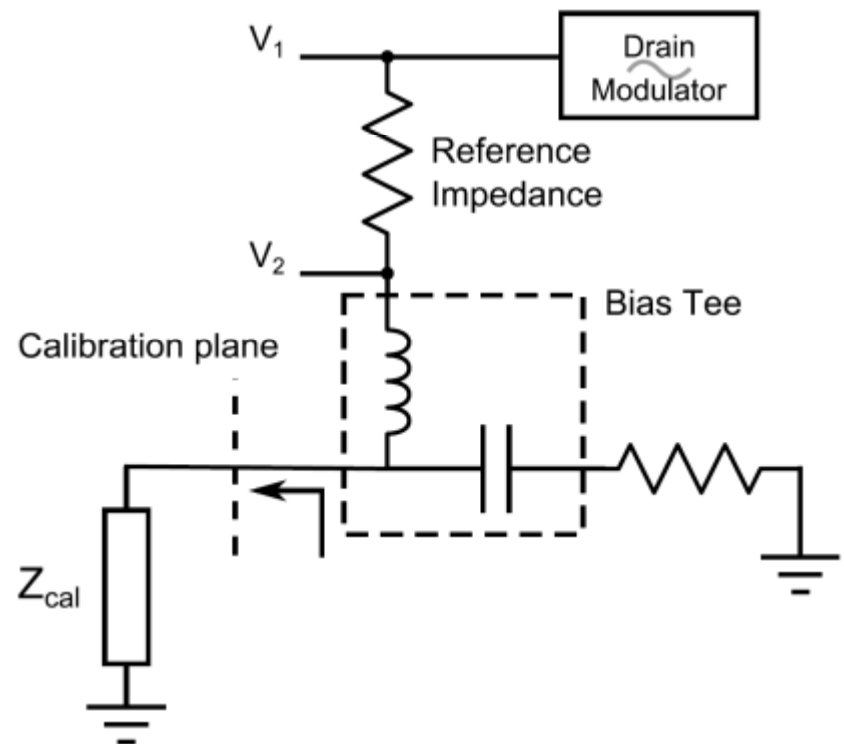
- Measurement setup is in progress

- Determine complex impedance by voltage waveforms with oscilloscope (V_1, V_2)

- Calibration allows measurement plane to be moved to transistor

Power Amplifier vs Transistor Impedance

Legend:
- Power Amp Re[Z_d]
- Power Amp Im[Z_d]
- Transistor Only Re[Z_d]
- Transistor Only Im[Z_d]

Y-axis: Impedance (Ω)
X-axis: Frequency (MHz)
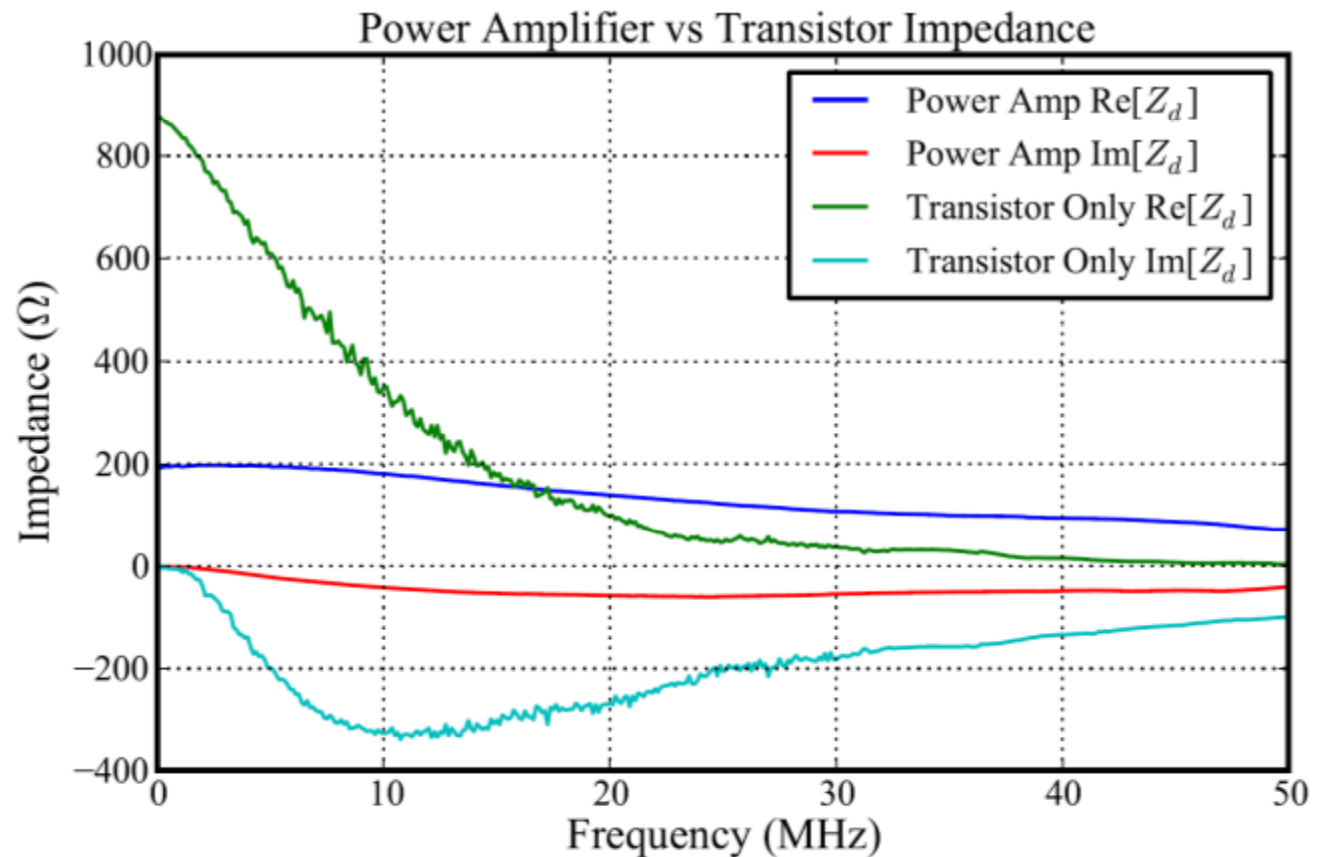
(Measurements taken on different devices biased with a similar drain current. No RF power was applied.)

Difference between PAs
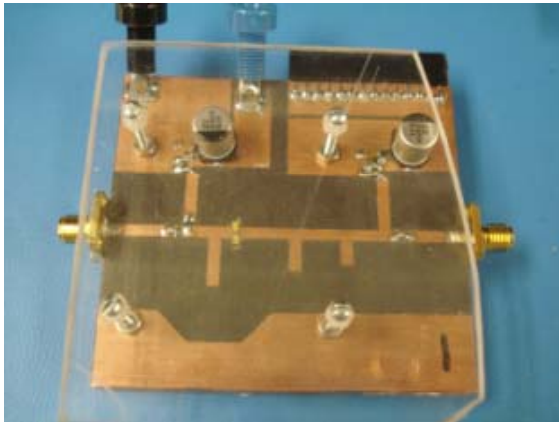
4-GHz PA
- I_d = 50 mA
- V_{dpk-pk} = 5 V
- P_{in} = 15 dBm
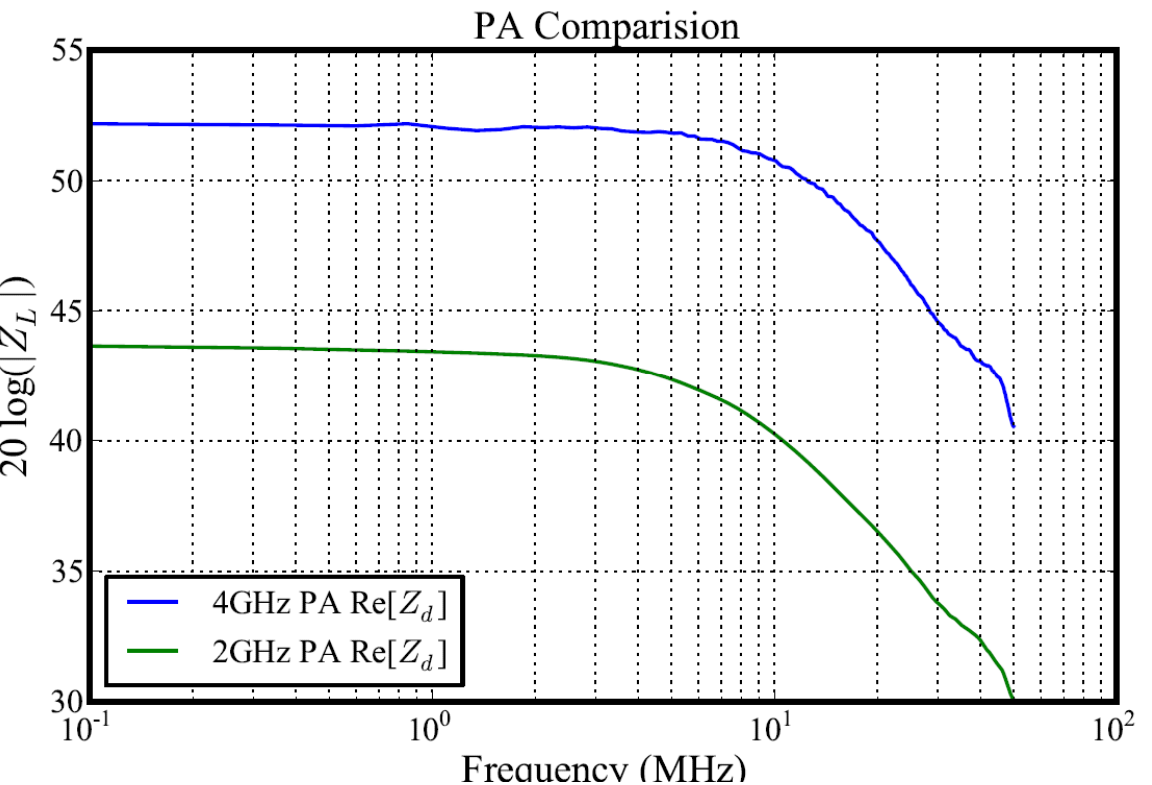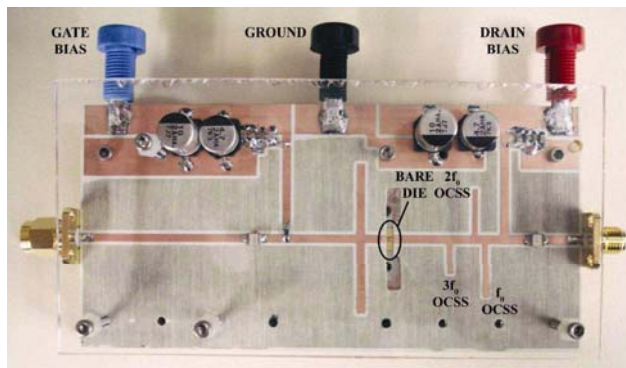
2-GHz PA
- I_d = 160 mA
- V_{dpk-pk} = 5 V

PA Comparision

Graph axes: $20 \log(|Z_L|)$ vs Frequency (MHz)

Legend:
- 4GHz PA Re[Z_d]
- 2GHz PA Re[Z_d]

X-band GaN MMIC PA
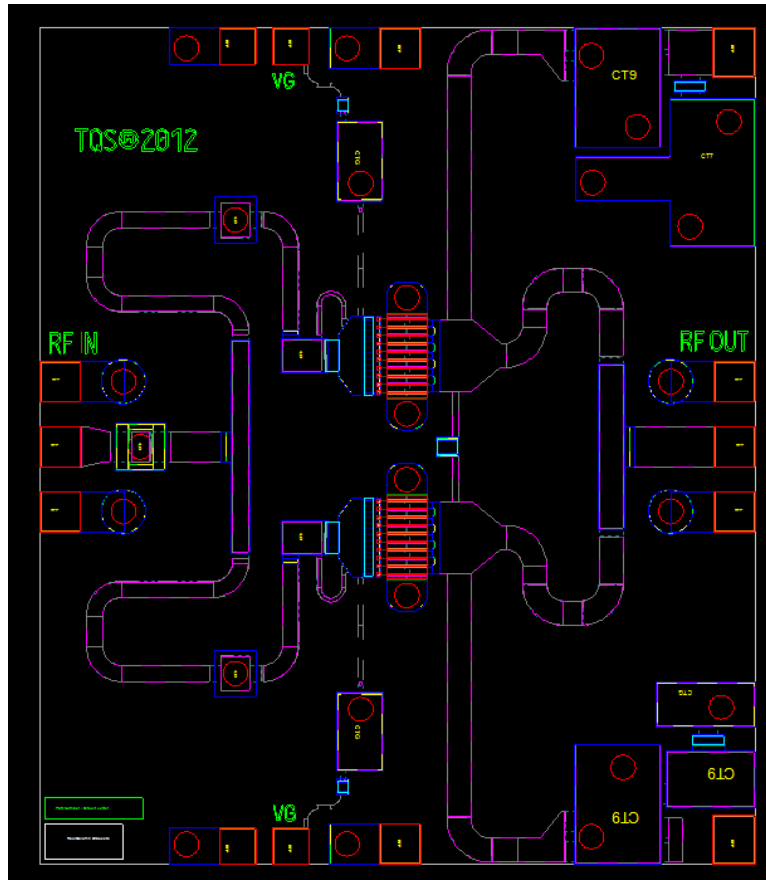
Single stage PA, two devices combined with a reactive combiner, devices are 10 fingers x100um
Total die size: 2.0mmx2.3mm
TriQuint 0.15um GaN process
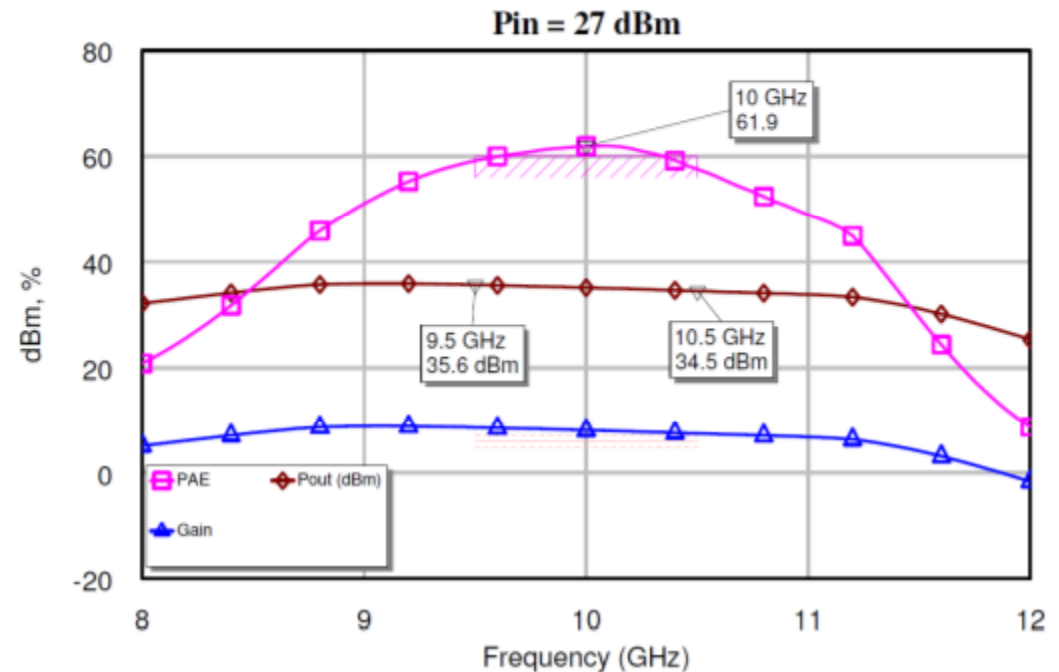
Drain Impedance Simulations

- Increasing bias decreases real and imaginary impedance (pinchoff to active)

- Increasing input power increases real impedance until saturation

f=15MHz
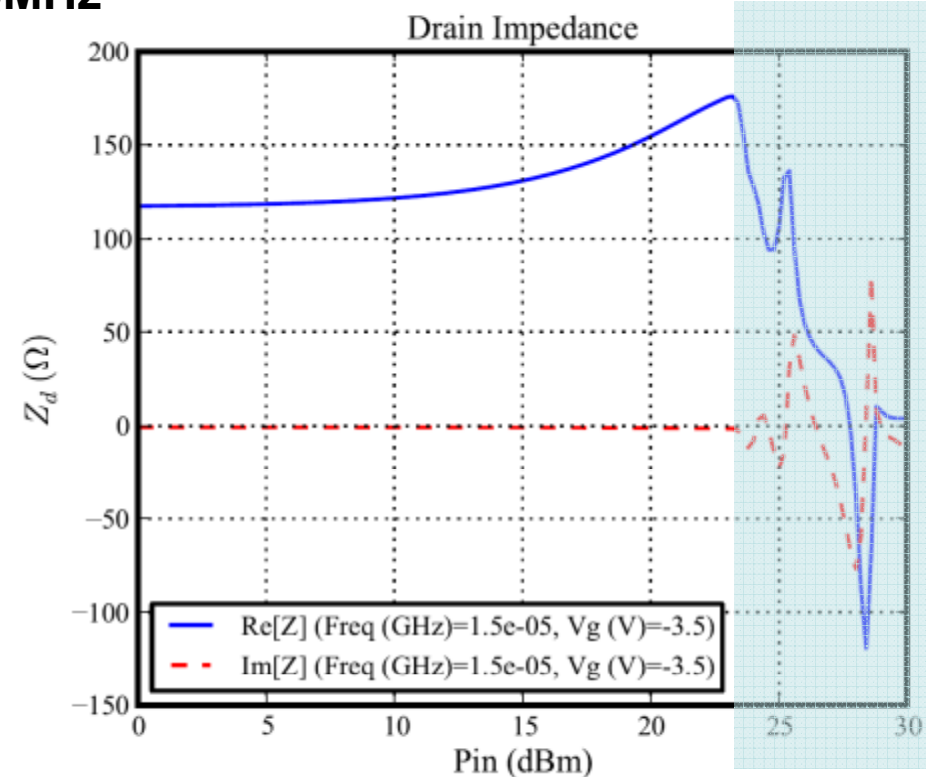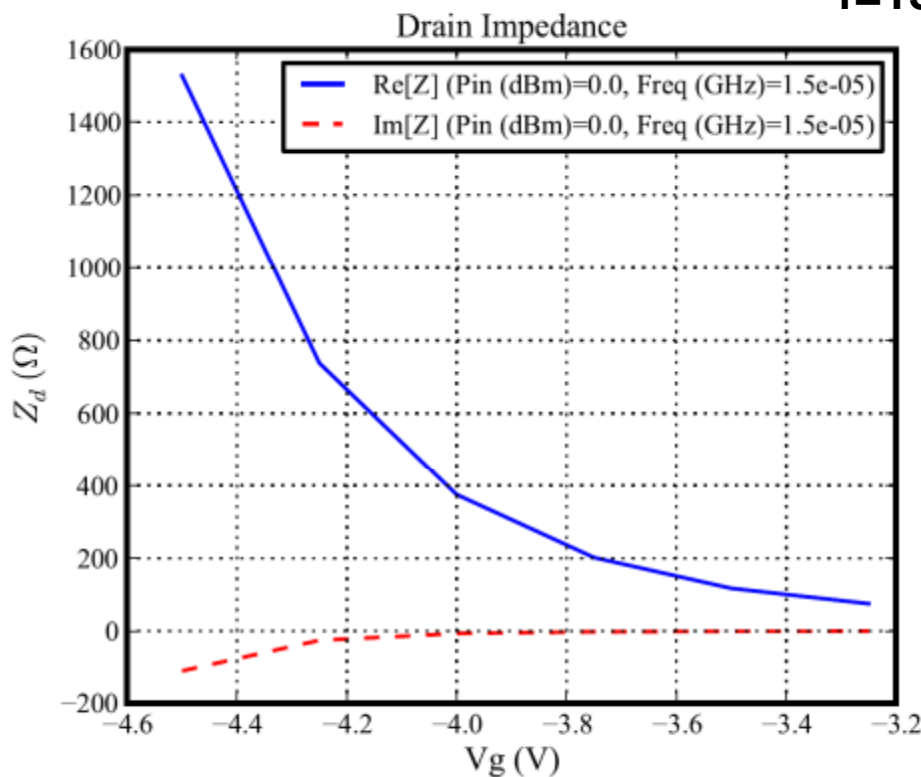
Drain Impedance Simulations

- While regions near top at high input power indicate negative real impedance
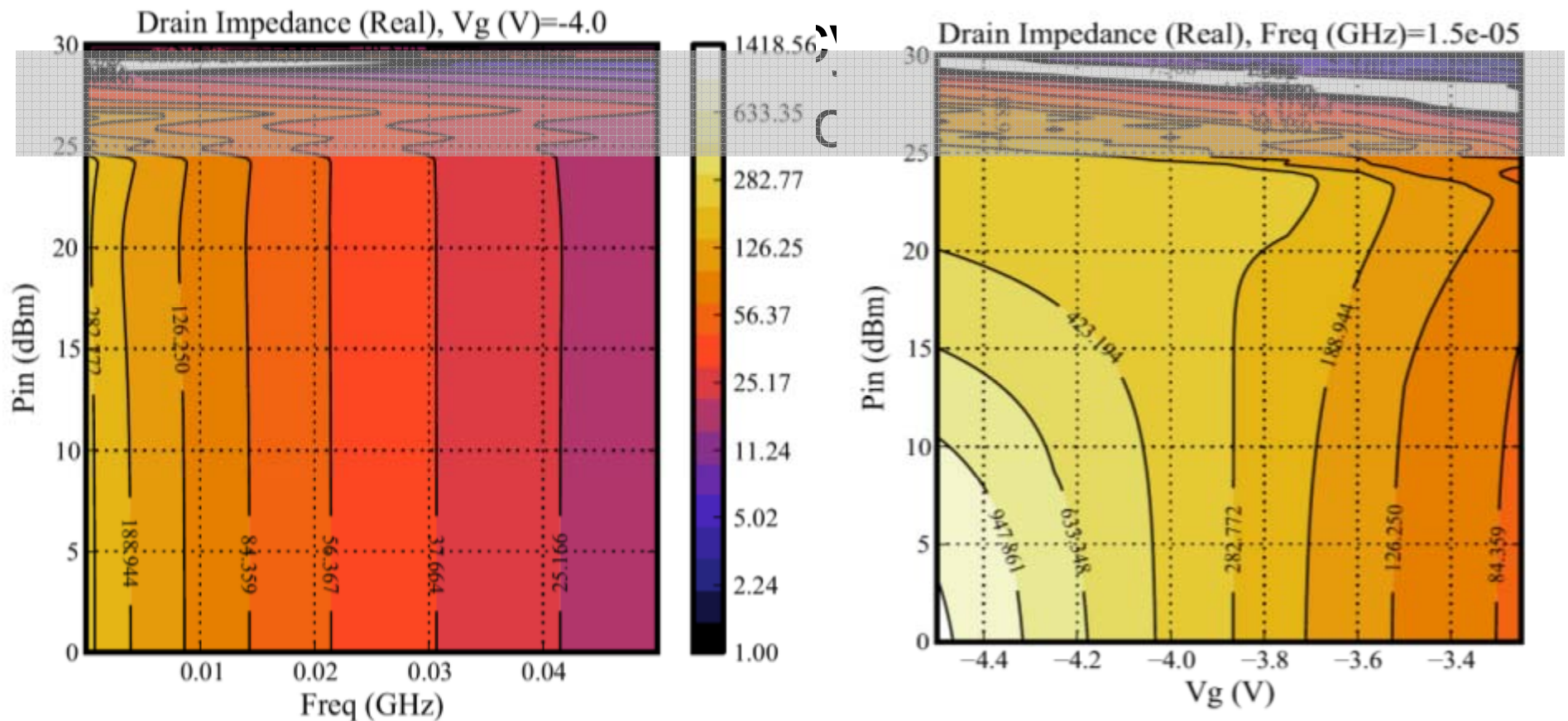
Single-ended X-band MMIC PA

Single stage single-ended,
10fingers x100um
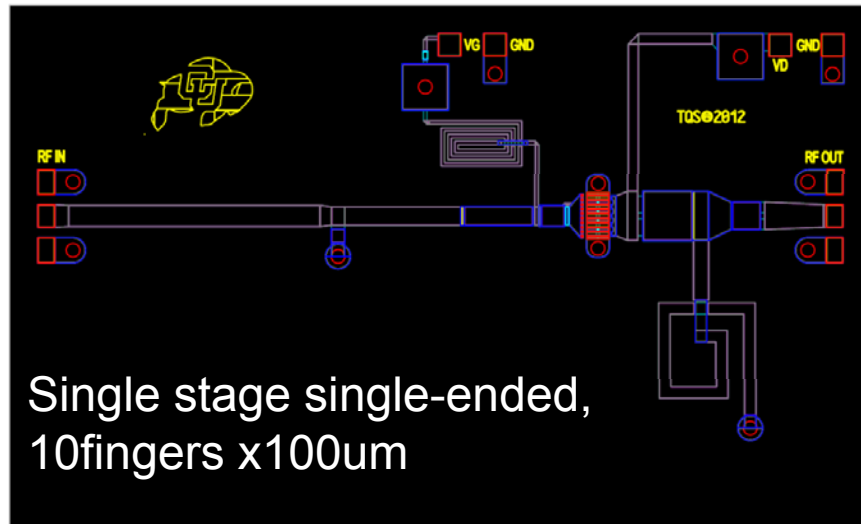
3.8mmx2.3mm
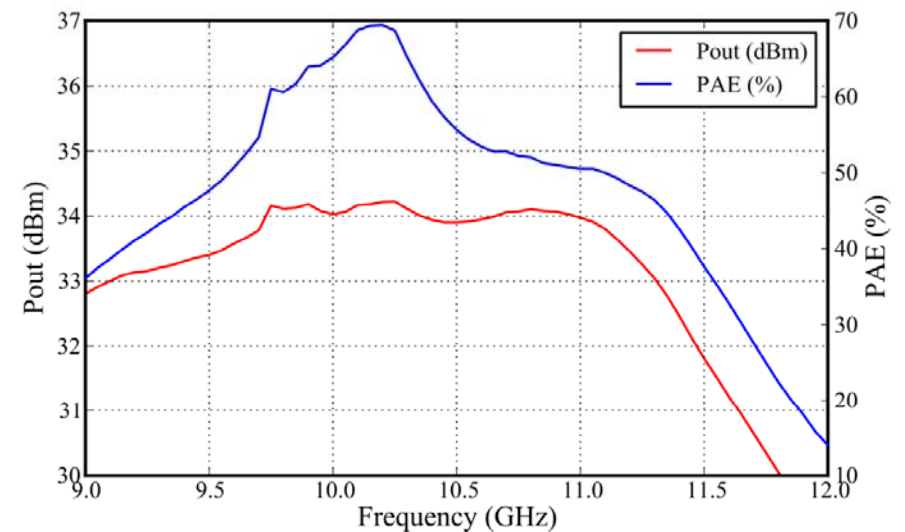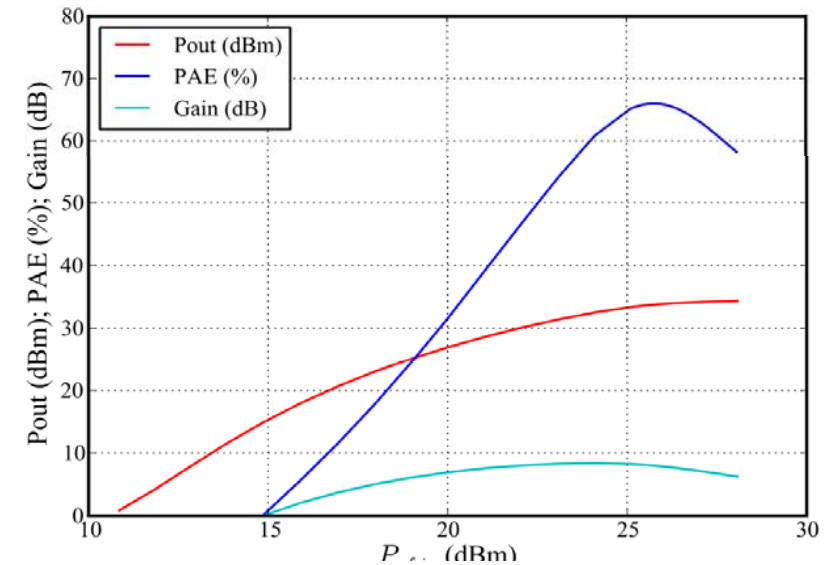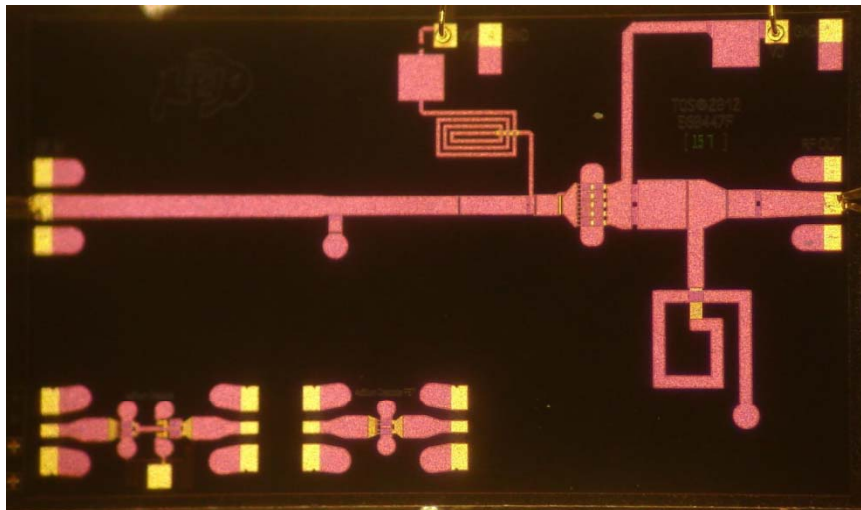
MMIC PA drain impedance measurements

f= 5 MHz

- Impedance increases before saturation
- Imaginary impedance approximately 0Ω
- High initial impedance in pinch-off
- Gain expansion visible in impedance

Legend:
- Meas Re[Z_d]
- Meas Im[Z_d]
- Sim Re[Z_d]
- Sim Im[Z_d]
- PAE (%)
- $P_{rf,out}$ (dBm)
- Gain (dB)
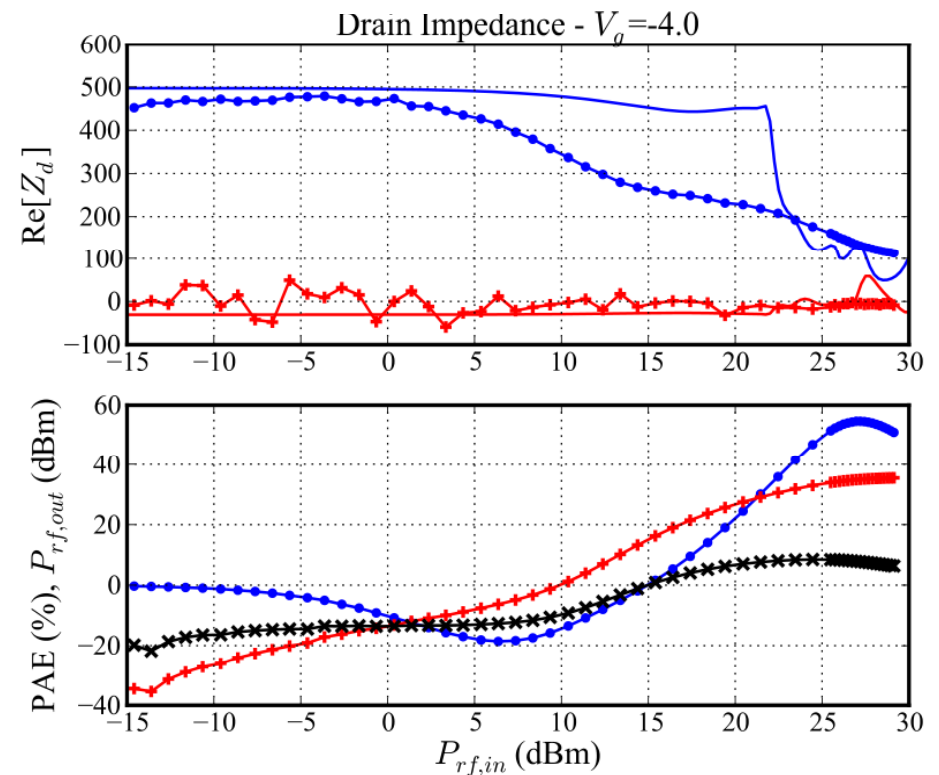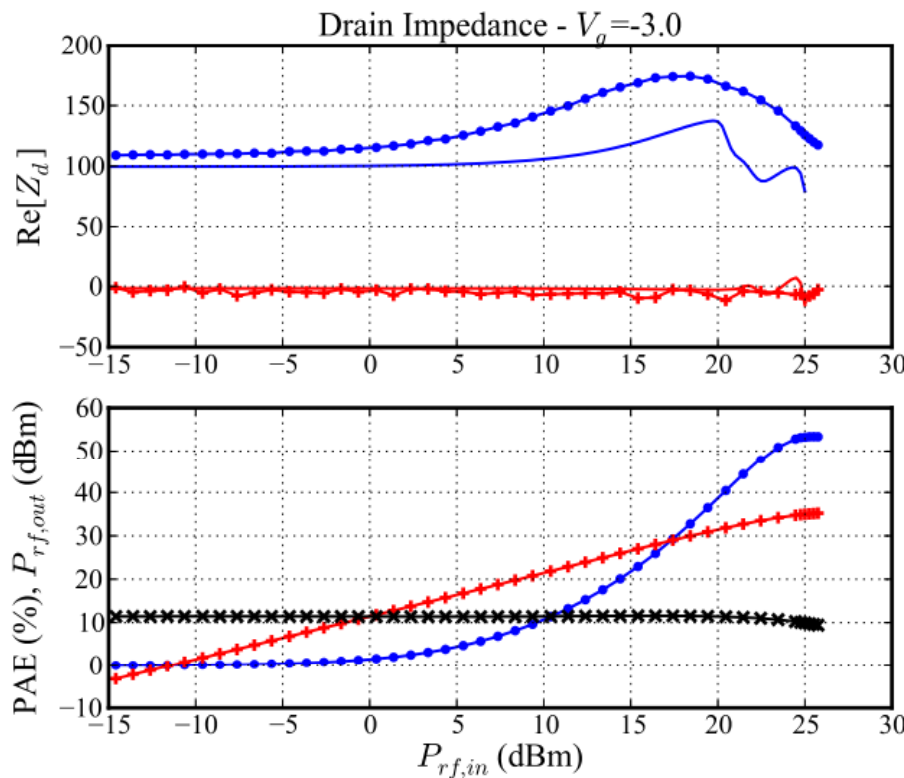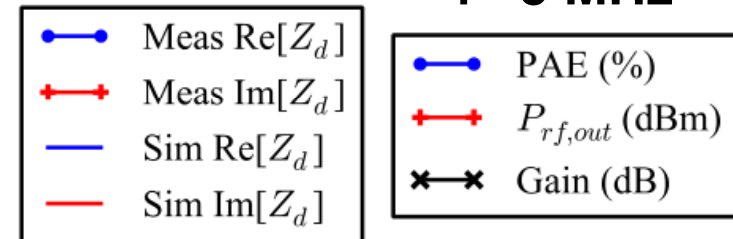
Conclusions about drain impedance measurements

- Variation of impedance at high modulation frequency is not negligible
  - Requires accurate characterization of transistor or accurate modeling.
- Accuracy of model at low frequencies with output saturation is debatable
- Calibration at low frequency is critical
- Good measured results and correlation with nonlinear device model can help design PA for SM/ET
- A linear very broadband supply modulator might be the best way to measure the dynamic drain impedance
- A low-frequency network analyzer is also an option

Supply issues:
Current Slew-Rate in an SMPS

Current Ramping Up

$+\Delta I_{Lsw}$

V_s+

Controller

L_{sw}

V_{out}

V_s-
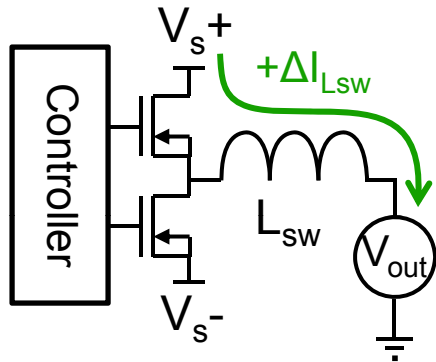
$$\frac{\Delta I_{Lsw}}{\Delta t} = \frac{V_S^+ - V_{out}}{L_{sw}}$$

Current Ramping Down

V_s+

L_{sw}

Controller

$-\Delta I_{Lsw}$

V_{out}

V_s-
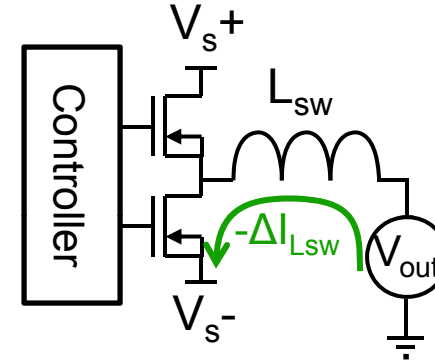
$$\frac{\Delta I_{Lsw}}{\Delta t} = \frac{V_{out} - V_S^-}{L_{sw}}$$

Slew rate determined by:

- inductance L_{sw}
- positive V_s^+ and negative V_s^- DC supply rails

Connection between SM and PA important

The figure shows a plot of Slew Rate [A/sec] (y-axis, 2×10^8 at top) versus Vdd [V] (x-axis, 0 to 70). Annotations include:
- Optimal Inductance = **163nH**
- Inductance too large (red line)
- Inductance too small (dark blue line)
- Maximum Supply, V_{sply}
- V_{off}
- $\frac{\Delta I_{Lsw}}{\Delta t} = \frac{V_s^+ - V_{out}}{L_{sw}}$
- $\frac{\Delta I_{Lsw}}{\Delta t} = \frac{V_{out} - V_s^-}{L_{sw}}$
- Instantaneous RFPA Drain Current Slew Rate vs. Voltage
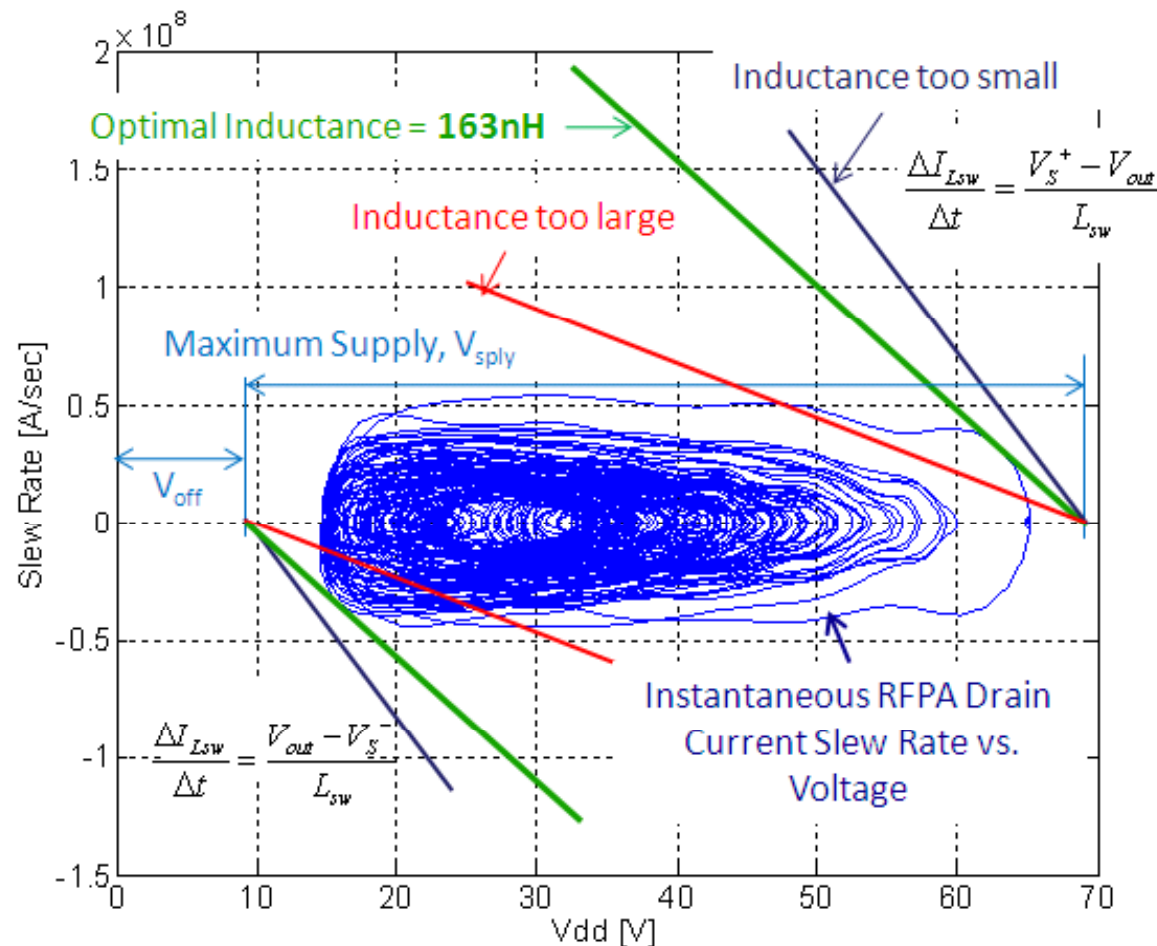
- For a given envelope waveform, required current slew rate is shown as a function of drain supply voltage

- V_s^+, V_s^- and the largest inductance L_{sw} that meets the worst-case slew-rate requirement

- Example: 2-carrier WCDMA, 6.8 dB PAR, 200W peak, 65V RFPA

L_{sw} = very small for high slew rate operation

Conclusions about SMPA low-frequency measurements

- Low-frequency important at input/output, but that can be characterized at baseband

- Non-standard measurements needed to characterize dynamic supply port impedance

- Good measurements and ultimate correlation with (new) models will allow for improved PA/SM co-design
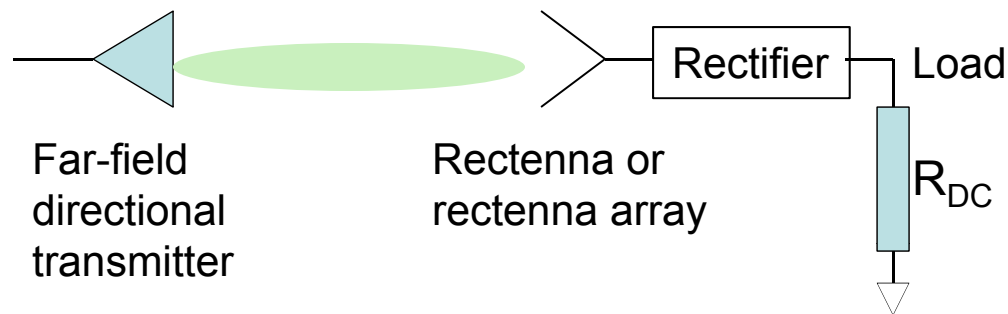
Motivation for rectifier measurements

Wireless power beaming

Far-field directional transmitter

Rectenna or rectenna array

Rectifier — Load

R_{DC}

- Wireless beaming vs. harvesting
- Modulate RF with LF to improve rectification efficiency
- Schottky diodes cannot handle high power
- Use transistors as rectifiers

Fast switching dc-dc converters
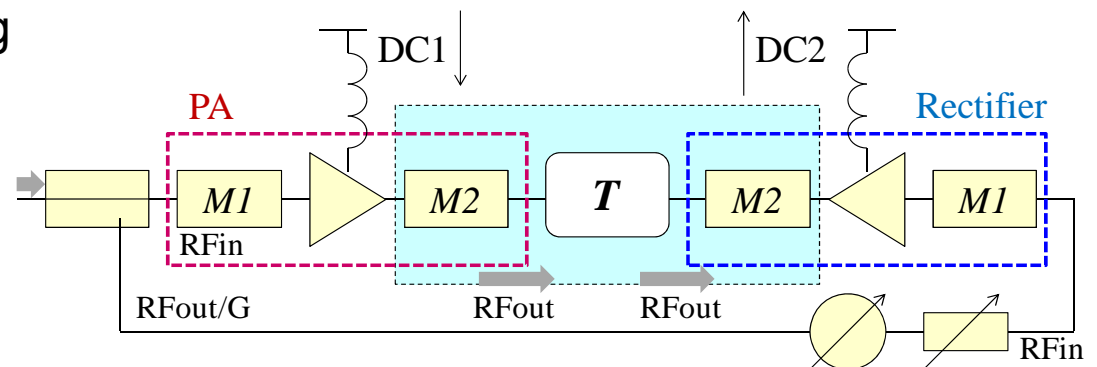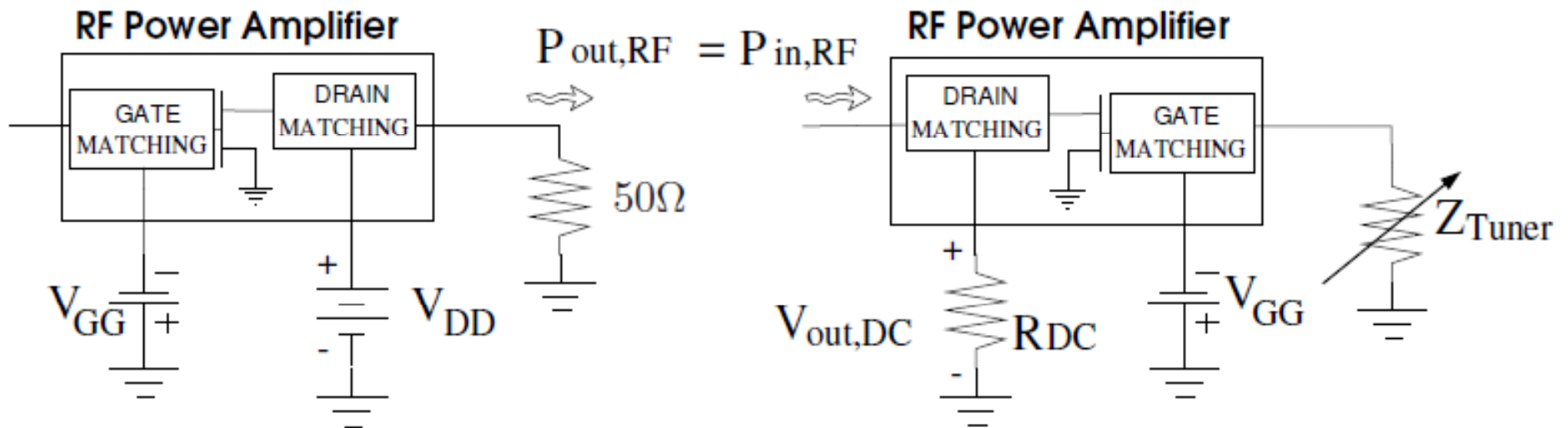
- Wireless beaming vs. harvesting
- Modulate RF with LF to improve rectification efficiency
- Schottky diodes cannot handle high power
- Use transistors as rectifiers

PA

DC1

DC2

Rectifier

M1   M2   T   M2   M1

RFin   RFout   RFout   RFin

RFout/G

Rectifier-PA duality

$$P_{out,RF} = P_{in,RF}$$

RF Power Amplifier — GATE MATCHING, DRAIN MATCHING, V_{GG}, V_{DD}, 50Ω

RF Power Amplifier — DRAIN MATCHING, GATE MATCHING, $V_{out,DC}$, R_{DC}, V_{GG}, Z_{Tuner}

High power conversion efficiency of a power amplifier (DC to RF) and a rectifier obtained by operating the amplifier in reverse (RF to DC) is achieved with time-reversal duality of the transistor's main current source. The power amplifier (PA) and rectifier (R) drain terminal voltage and current are related by

$$v_{PA}(t) = v_R(t) \qquad i_{PA}(t) = -i_R(t)$$

Hamill, D.C.: 'Time Reversal Duality and the synthesis of a double class E DC-DC converter', 21st Annual IEEE Power Electronics Specialists Conference, 1990, pp. 512-521

Class-F PA and Rectifier Simulations

- Simulations performed with a 8x75um GaN HEMT model at 2.14GHz
- The nonlinear model includes:
  - Nonlinear Cgs, Cgd, Cds
  - Gate-source and gate-drain diodes
  - Breakdown modeling
  - Trapping effect modeling
- Model reproduces nonlinear behavior for positive and negative drain voltages
- For PA, consider drain efficiency as metric

$$\eta_{PA} = \frac{P_{out,RF}}{P_{DC}}$$

- In class-F, 5 harmonics terminated
- Vds=28V, Vgs=-4.9V, obtained efficiency of 72%
- Observe I-V curves and load-line, and V,I waveforms and compare to rectifier

Callet, G., Faraj, J., Jardel, O., Charbonniaud, C., Jacquet, J.C., Reveyrand, T., Morvan, E., Piotrowicz, S., Teyssier, J.P. and Quéré R.: 'A new nonlinear HEMT model for AlGaN/GaN switch applications', Intern. Journal of Microwave and Wireless Techn., 2010, 2, (3-4), pp. 283-291

Class-F PA and Rectifier Simulations

- Simulations performed for rectifier mode with the same 8x75um GaN HEMT model at 2.14GHz
- Drain supply replaced by Rdc
- The input is now RF power $P_{inRF}=P_{outRF}$ of the amplifier, injected in drain port
- Assuming DC gate current is negligible, the RF-DC conversion efficiency given by

$$\eta_R = \frac{P_{DC}}{P_{in,RF}} = \frac{2|V_{DC}|^2}{R_{DC}\Re\{V_{drain}(f0)I^*_{drain}(f0)\}}$$

- In class-F, 5 harmonics terminated
- Pin=, Vgs=-4.9V, obtained efficiency of 80% with Rdc=120Ω
- Observe I-V curves and load-line, and V,I waveforms and compare to rectifier
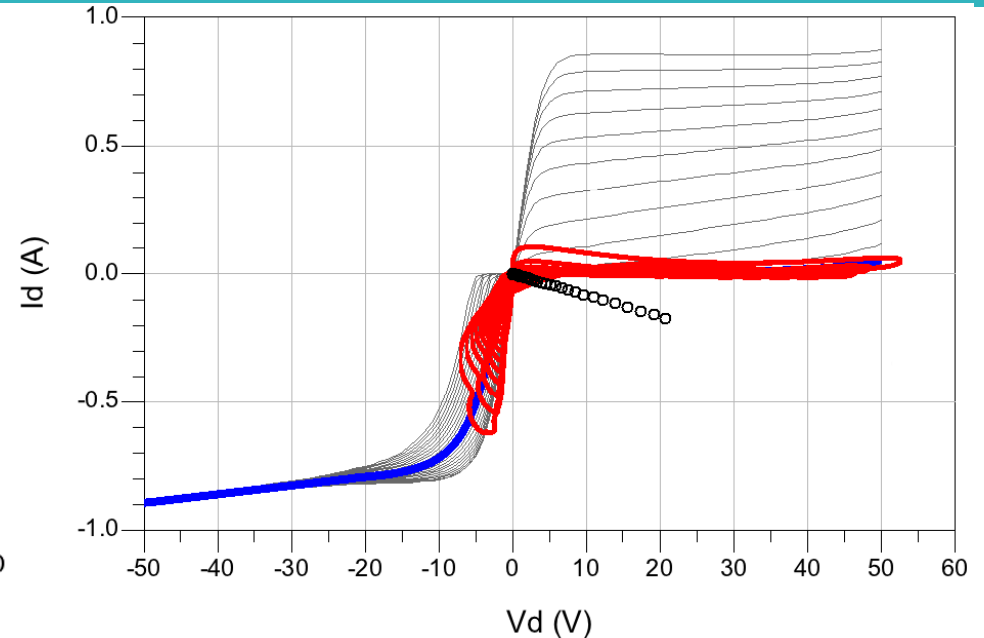
PA-rectifier time reversal
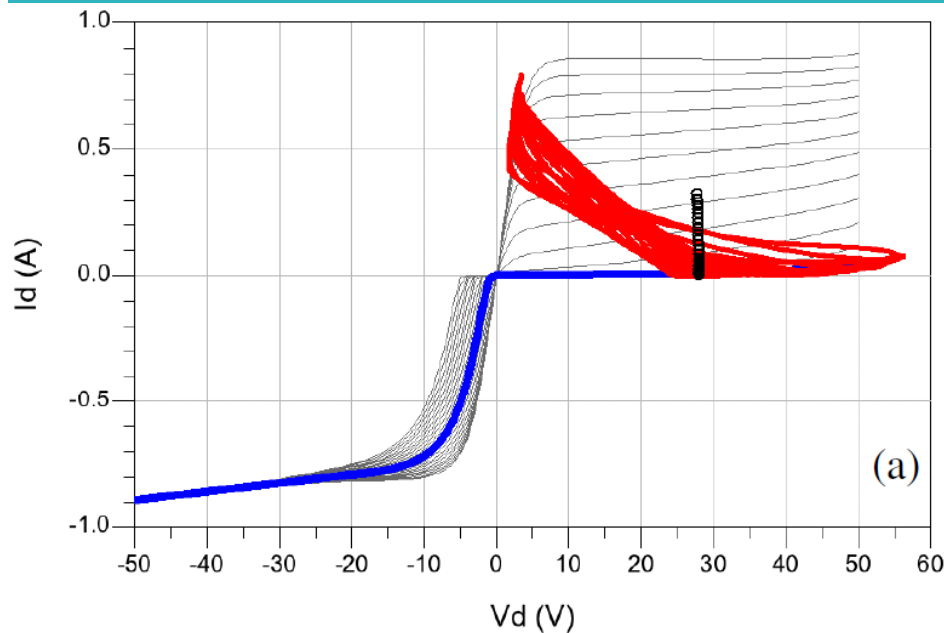
(a)

Simulated GaN transistor I-V curves (gray), dynamic load lines (red) and drain DC voltage and current (black) for the PA

The blue line is the Vgs=-4.9V transistor characteristic (the gate bias point value)

Vdd=28V, Power swept from 0-40dBm

Simulated GaN transistor I-V curves (gray), dynamic load lines (red) and drain DC voltage and current (black) for the rectifier

The blue line is the Vgs=-4.9V transistor characteristic (the gate bias point value) Time-reversal duality is seen at 2.14 GHz.

Simulated time domain waveforms

Simulated GaN transistor time domain intrinsic drain voltage (blue) and current for the power amplifier with Vds=28V, as the output power is swept from 0-40dBm

Simulated GaN transistor time domain intrinsic drain voltage (blue) and current for the rectifier as the power is swept from 0-40dBm
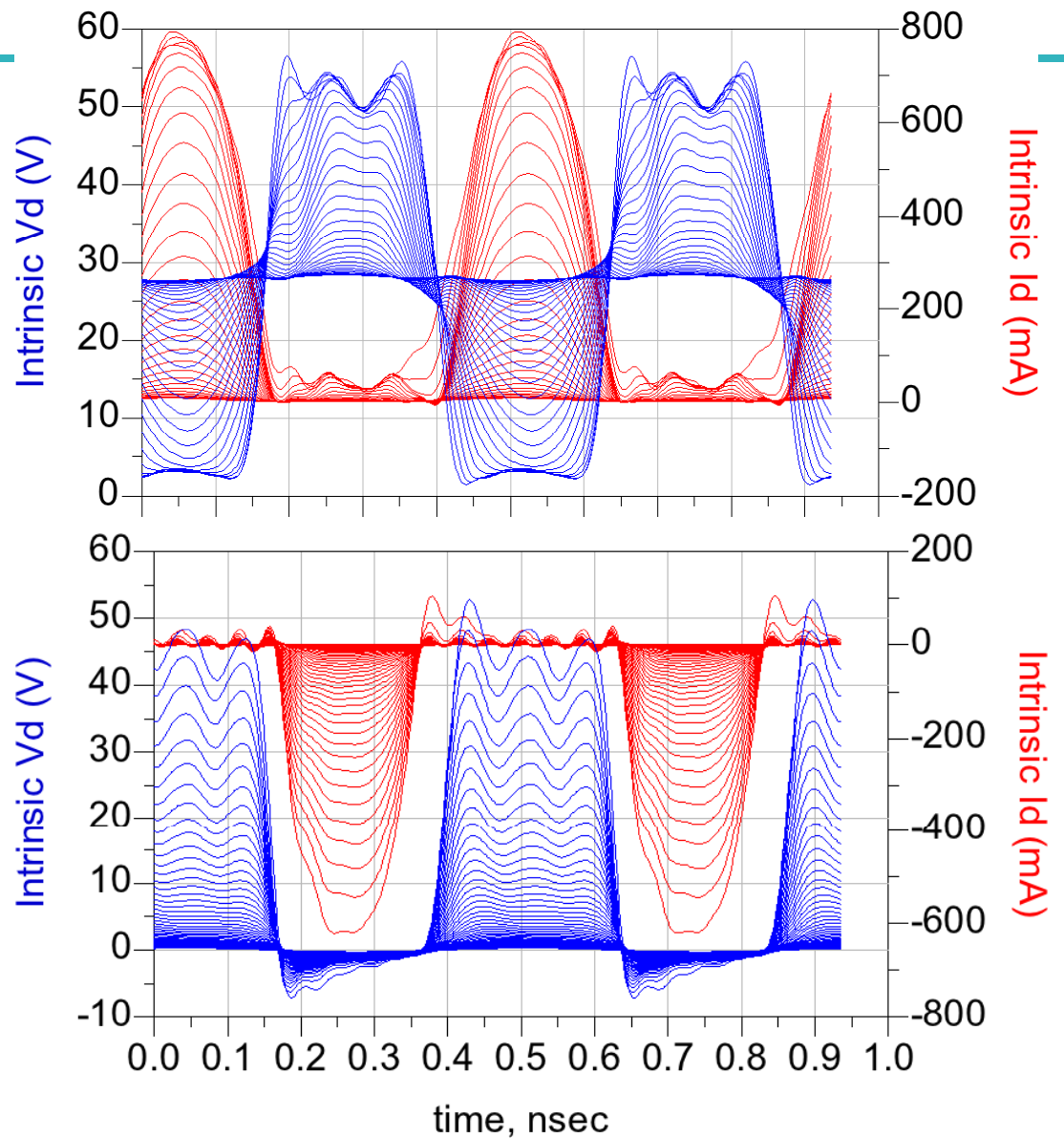
Simulated load pull

Simulated Class-F GaN transistor rectifier gate-port load-pull contours
- Optimal impedance for conversion efficiency at 2.14GHz shown
- Related to dynamic load-line with minimal enclosed area
- Close to the I-V characteristic at constant Vgs
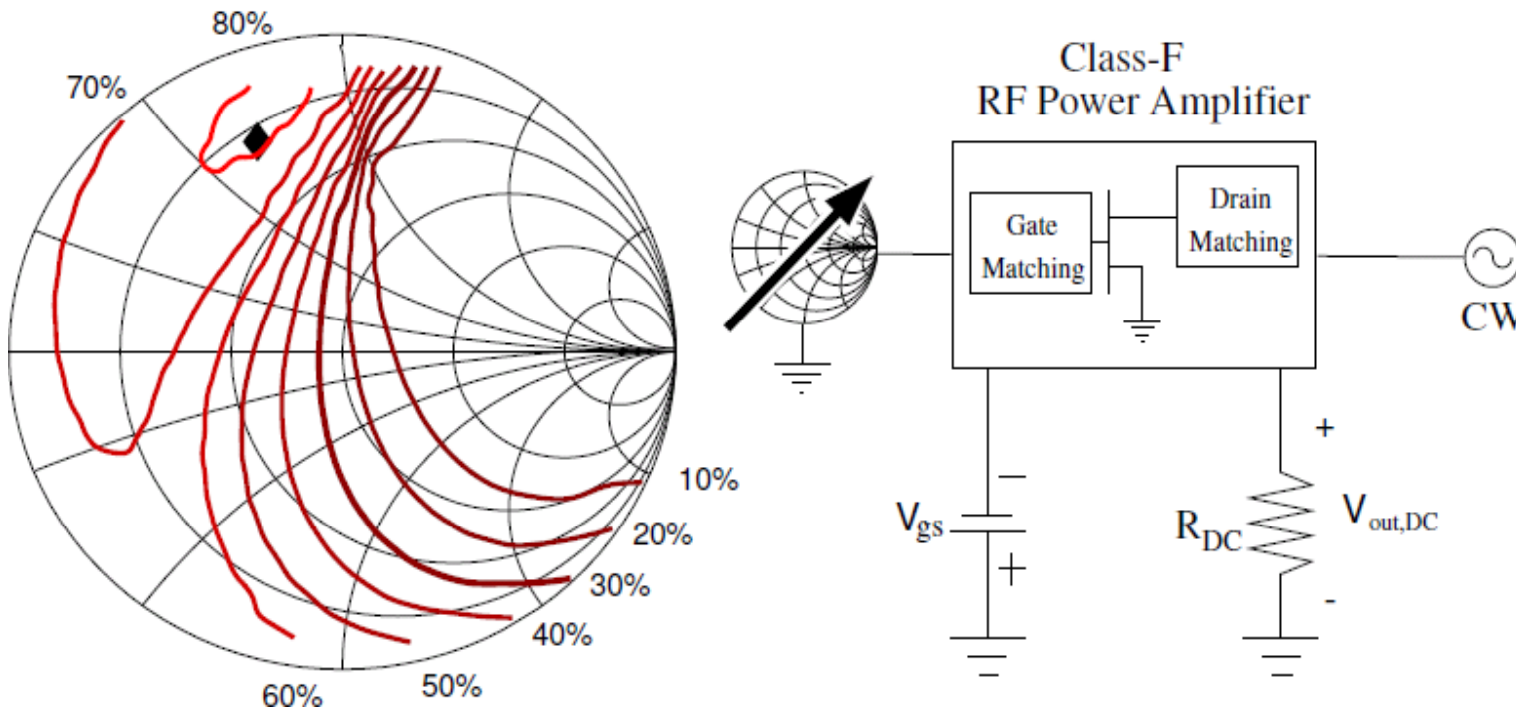
Reveyrand, T., Ramos, Popovic, Z. "Time-reversal duality of high-efficiency RF power amplifiers," IET Electronics Letters, Dec.6 2012
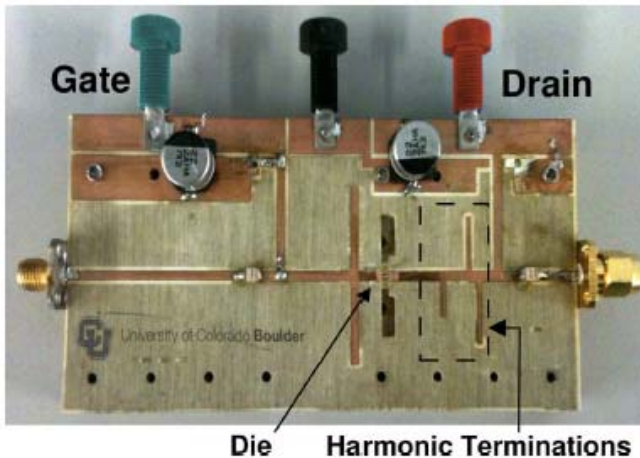
Rectifier efficiency

Rectifier performance measured at the coaxial reference planes at f=2.14 GHz.
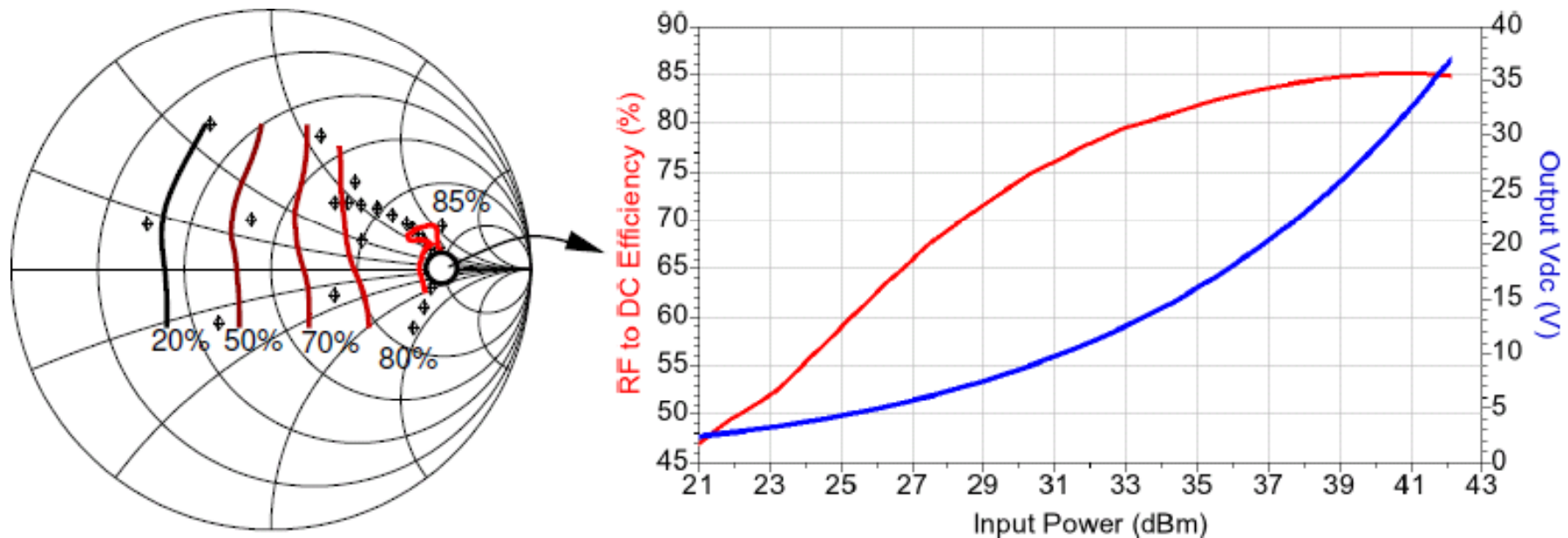
RF load impedances used for measurements (black dots), where the contours correspond to max efficiency for the complete power sweep applied to the RF drain port.
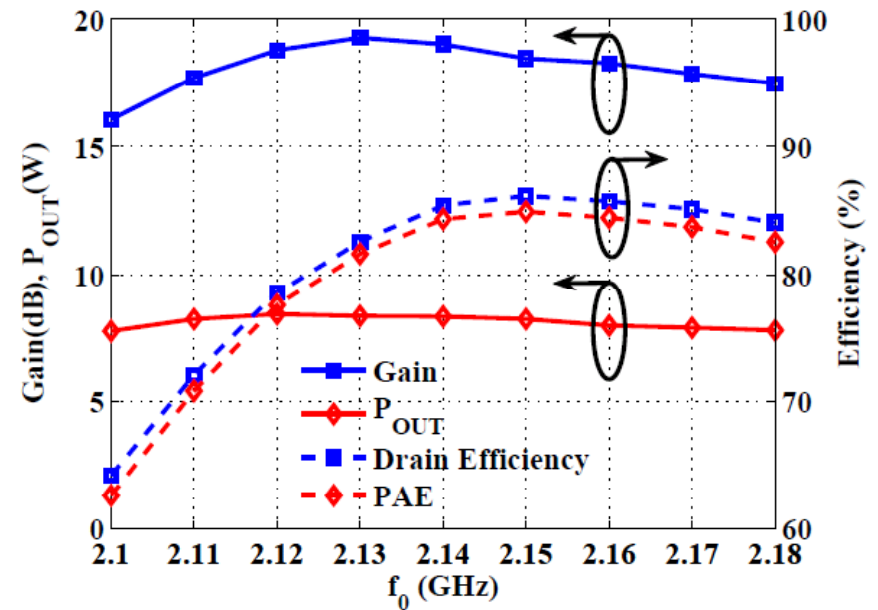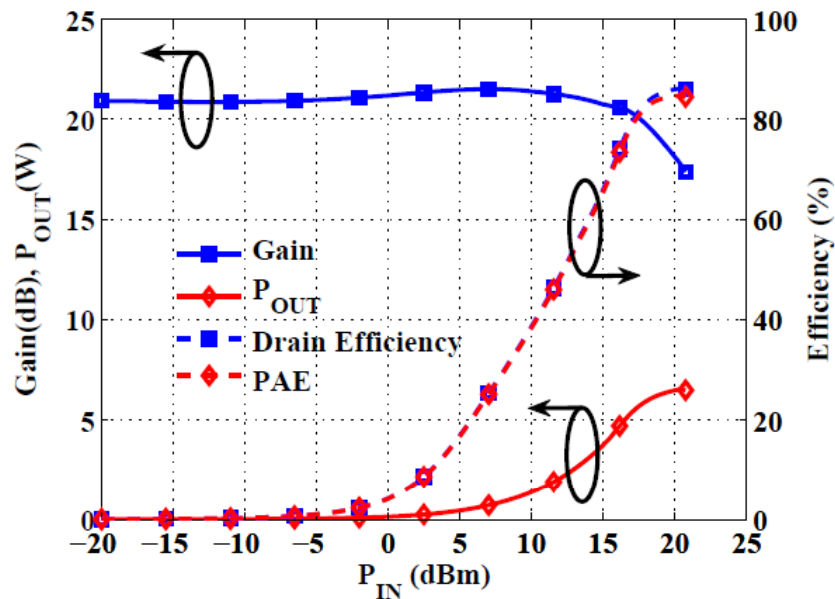
V_{DC} and efficiency measured for R_{DC} =98Ω and Zload = (229 + j0.9)Ω.

Measurements: Class F⁻¹

Class-F-1 power amplifier
based on TriQuint TGF2012 GaN 12-W die
Pout=7W at f=2.14GHz
PAE=84.6% at Vdd=31V with G=19dB
(published)

Roberg, M., Hoversten, J., and Popovi´c, Z.: 'GaN HEMT PA with over 84% power added efficiency', Electronics Letters, 2010, 46, (23), pp. 1553-1554
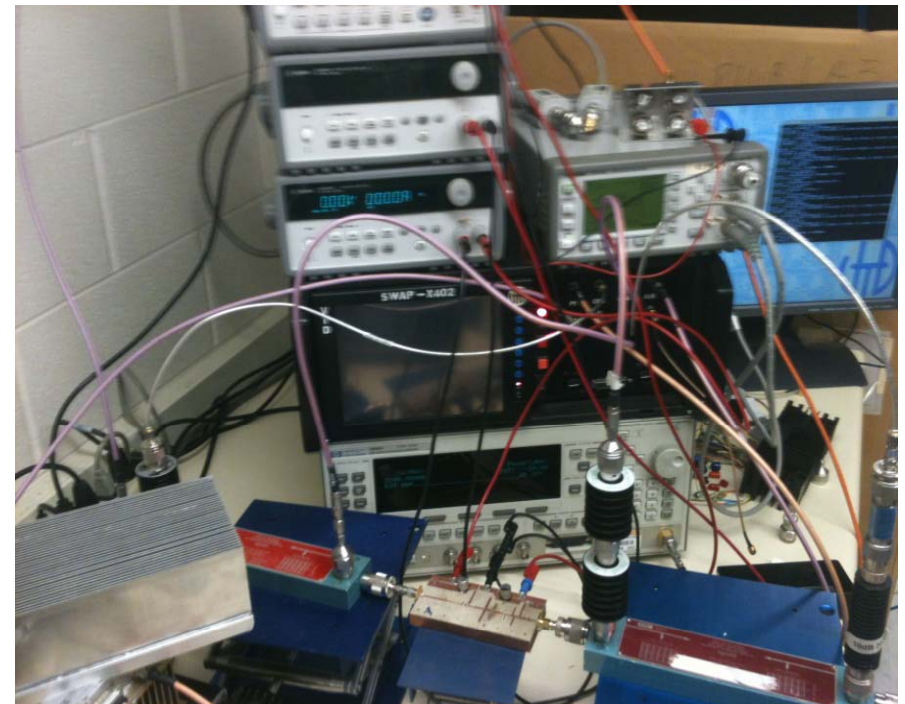
PA measured as rectifier

- An RF power sweep is performed at the input drain port for each RF impedance provided by the tuner at the gate port
- The output DC power delivered to the load RDC is calculated from the DC voltage as measured by a voltmeter
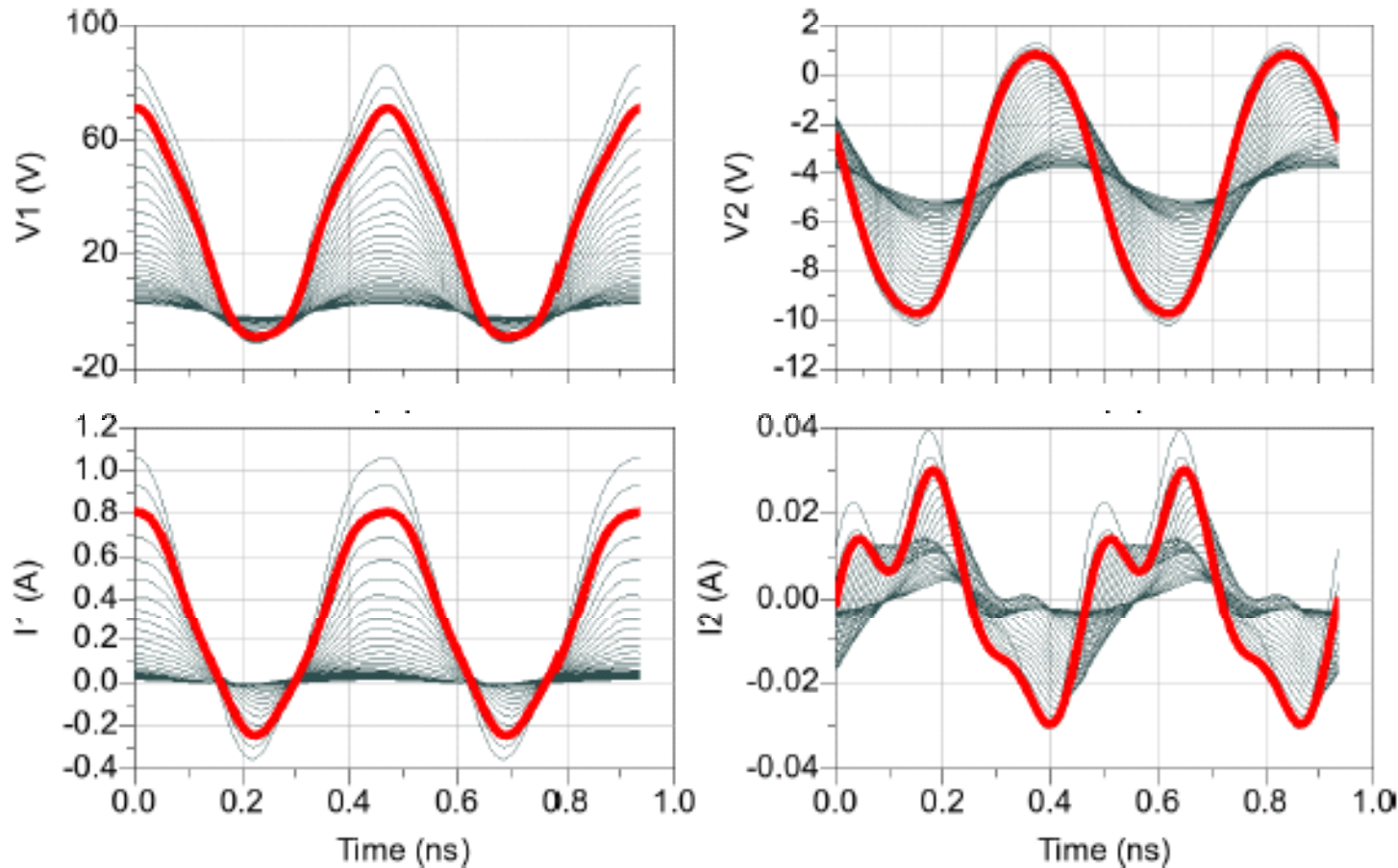- Time-domain measurements
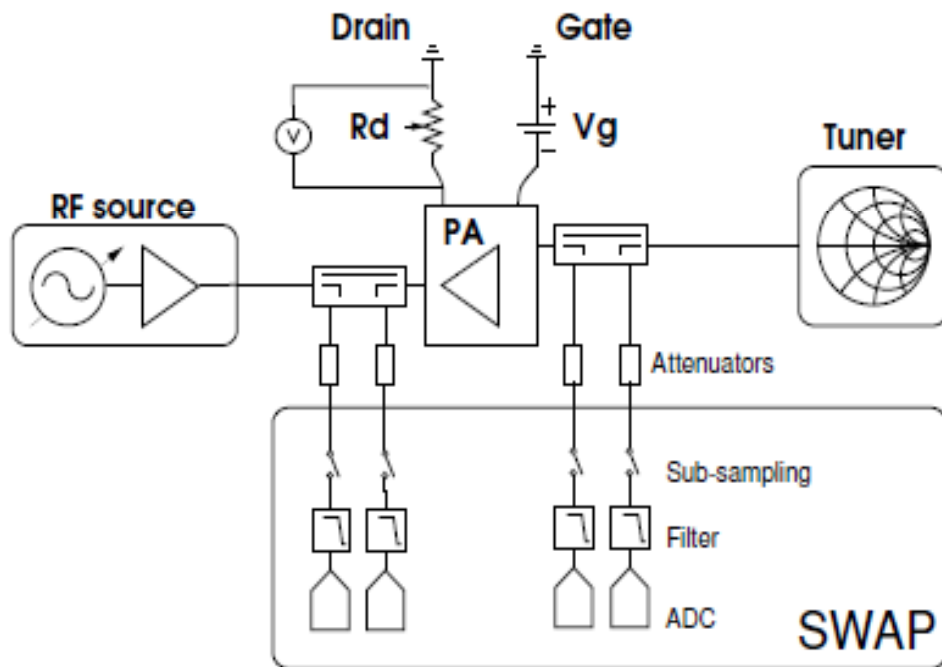
Rectifier load-pull measurement setup

Measured time-domain waveforms
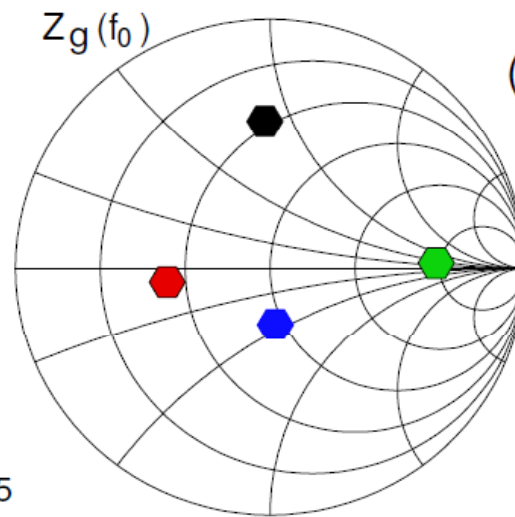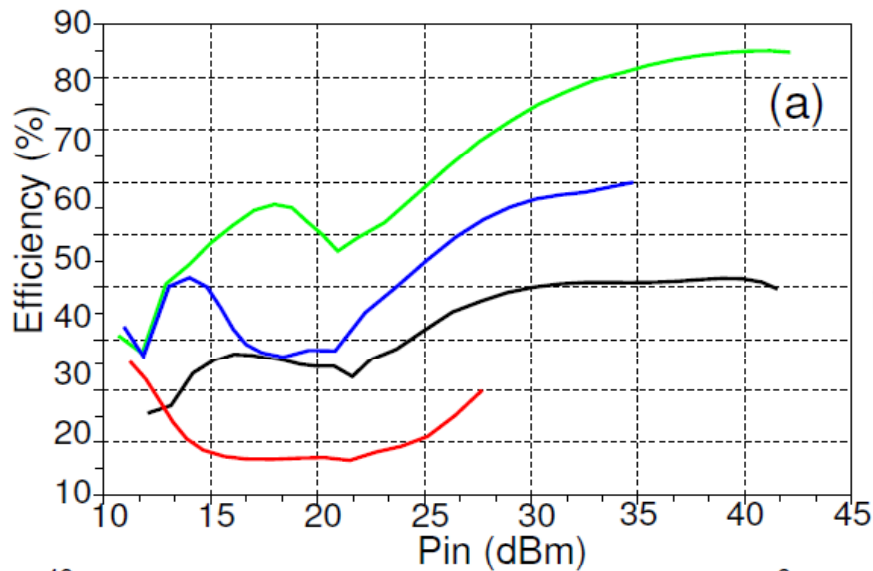
There is a gate signal with no gate input:

Self-synchronous operation
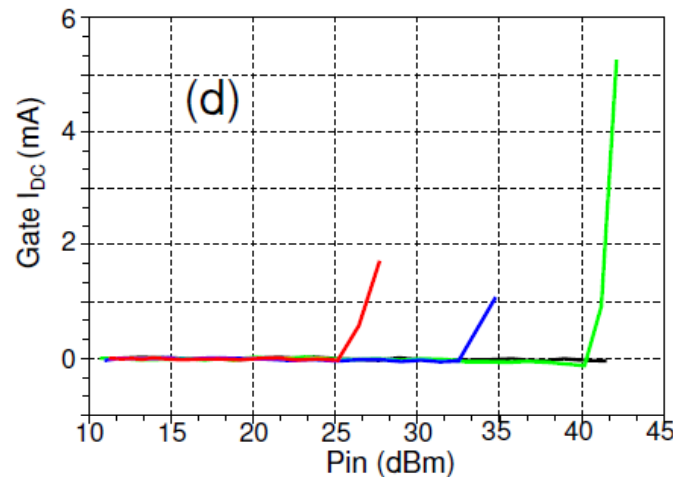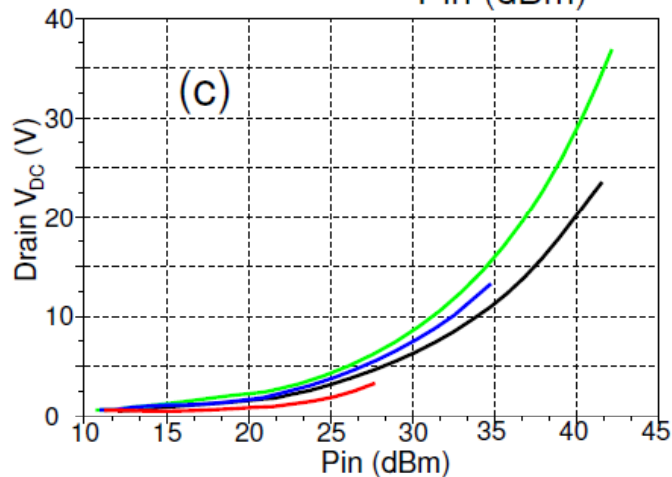

V_{gs}= -4.4 V
R_{dc}= 98.5 Ω
$Zg(f_0)$= 230 +j0.1Ω

V2 and I2 are signals coupled to the gate matching network through Cgd.
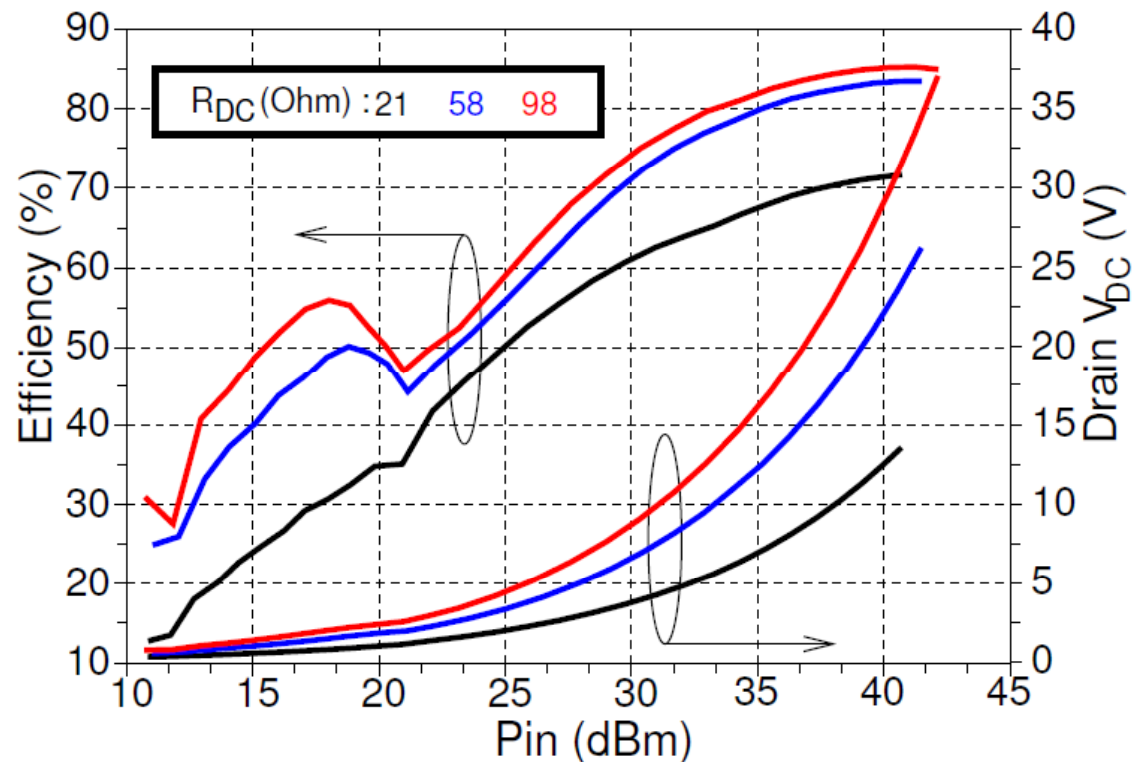
Measured efficiency and output voltage

- Efficiency greatly influenced by gate impedance
- η_{max} = 85 %
- P_{in} = 42 dBm
- V_{dc} = 36 V
- Low gate impedance causes gate diode to conduct earlier

Rectifier conversion efficiency measurements

- Efficiency is greatly influenced by DC load
- High efficiency achieved at high input power and high output voltage

$Vg = -4.4$ V, $Zg(f_0) = 230 + j10$ Ω

$\eta_{max} = 85$ % with $P_{in} = 40$ dBm and $R_{dc} = 98$ Ω

Roberg, M., et al., "High-Efficiency Harmonically-Termindated Diode and Transistor Rectifier," Microwave Theory and Techniques, IEEE Transactions on , (Accepted)
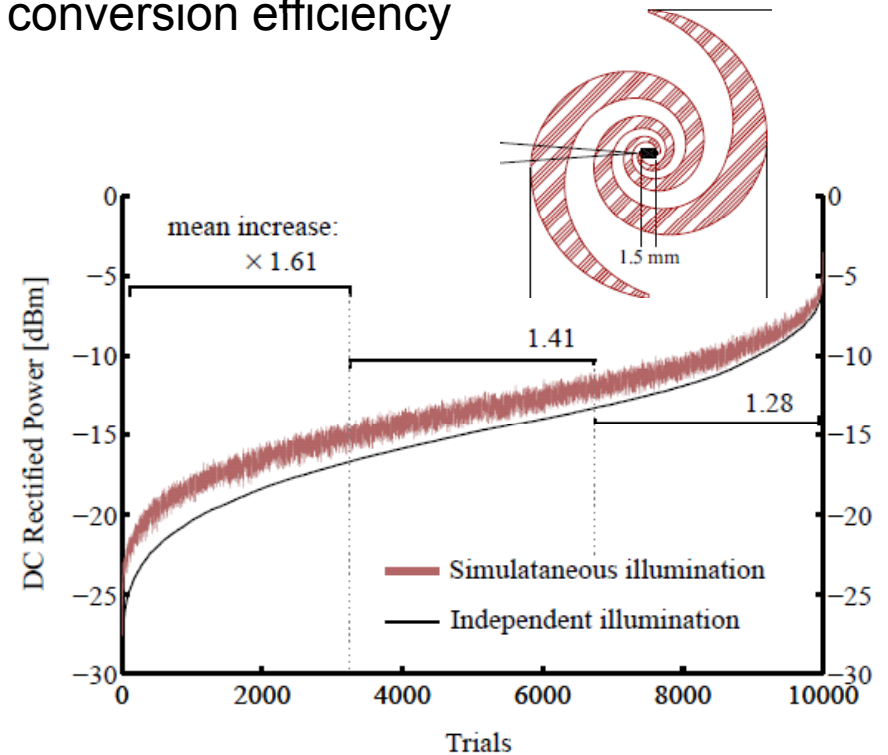
LF modulation of input RF for rectifiers

Modulate input frequency or PWM to control output DC voltage in DC-DC converter

Modulate input frequency (multi-tone excitation) in order to improve conversion efficiency
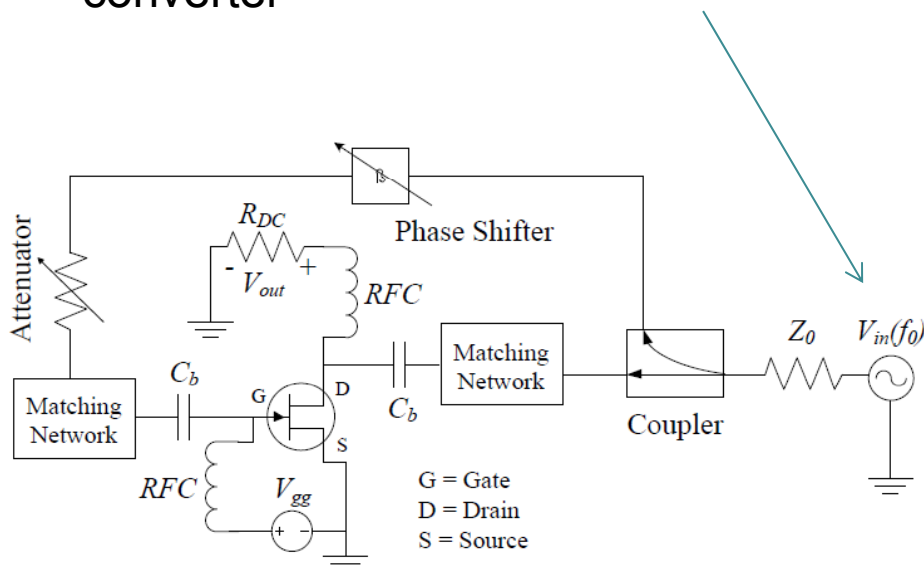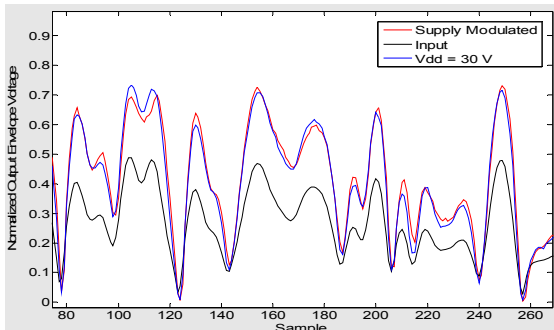

"A UHF Class E2 DC/DC Converter using GaN HEMTs," R. Marante, N. Ruiz, L. Rizo, L. Cabria, J. A. García, IEEE T-MTT, Dec. 2012

J.A Hagerty, F.B. Helmbrecht, W. McCalpin, R. Zane, Z. Popovic, "Recycling ambient microwave energy with broadband rectenna arrays," 2004.

Conclusions

- Low-frequency measurements for microwave circuits are not well established or understood
- Currently, very expensive microwave oscilloscopes, or specialized nonlinear network analyzers are the only option
- There is a need for time-domain measurements that can handle very different time scales
- Simultaneous low and high-frequency measurements allow for new circuit approaches and designs
- In this talk, we showed some challenges in envelope-frequency transistor and PA measurements for high efficiency transmitters and rectifier measurements for power applications

Thank you !