

# First Demonstration of AlInN/GaN HEMTs Amplifiers at K band

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**Abstract** — AlInN/GaN HEMTs have shown outstanding power performances for high frequency applications, due in particular to their high current densities and their thinner barrier layers than in AlGaIn/GaN HEMTs that minimize short channel effects. In this paper, we present the first published power results of two K-band hybrid amplifier demonstrators at 20GHz and 26.5GHz using 0.25 $\mu$ m gate length devices. At these frequencies, respectively, cw RF output power of 4.5 Watts with 20% PAE and 1.65 W with 15.5 % of PAE were obtained. These state-of-the-art results confirm the potential of AlInN/GaN technology for high frequency applications.

**Index Terms** — AlInN/GaN HEMTs, K band power amplifiers.

## I. INTRODUCTION

AlInN/GaN HEMTs are considered as an interesting alternative to AlGaIn/GaN HEMTs in several laboratories. Since few years, this technology is in development and already outstanding power performances have been reached [1-4]. What appeared recently is that the advantage of AlInN/GaN HEMTs over AlGaIn/GaN HEMTs can be particularly remarked at high frequencies of operation [4-6]. After a brief description of the epitaxial and technological process of the devices, we will show in this paper the first demonstration of amplifiers using relatively long 0.25 $\mu$ m gate length AlInN/GaN HEMTs, for frequencies of operation of 20GHz and 26.5GHz. The good results obtained confirm the interest for such heterostructure.

## II. OVERVIEW OF THE EPITAXIAL AND TECHNOLOGICAL PROCESSES

The structure of an AlInN/GaN power HEMT from the wafer used for the fabrication of the amplifiers is presented at Fig. 1. The layers are grown on SiC substrate by Low Pressure Metal Organic Chemical Vapour Deposition (LP-MOCVD) using a 2-inch single wafer reactor. The heterostructures consist in a 1.7 $\mu$ m insulating GaN buffer layer, a 1nm thick AlN spacer layer and an 11.5nm thick undoped AlInN layer with 18.7% of Indium content, giving rise to lattice matched GaN buffer and barrier AlInN layers.

The sheet resistance and the sheet carrier density are evaluated respectively at 311 $\Omega$  and 1.3.10<sup>13</sup> cm<sup>-3</sup>. Ohmic contacts are

formed by rapid thermal annealing of Ti/Al/Ni/Au multilayer at 900°C during 30s under nitrogen ambient, and show an average resistance of 0.15 $\pm$ 0.02 $\Omega$ .mm. Argon ion implantation is used for device isolation. 250nm Ni/Pt/Au T-gates are obtained by e-gun evaporation after electron beam lithography. The devices are passivated with a 250nm thick Si<sub>3</sub>N<sub>4</sub> layer deposited by plasma enhanced chemical vapour deposition. A Ti/Pt/Au multilayer deposited by e-gun is used for interconnections. Multifinger device 3D interconnects are fabricated with plated gold bridge technology on photosensitive BCB.

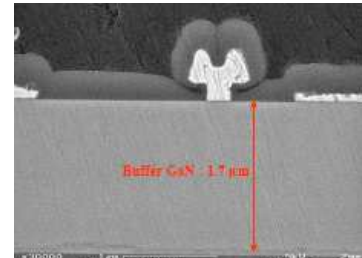


Fig. 1. Microsection of the active area of a 0.25 $\mu$ m AlInN/GaN HEMT from the considered wafer. The source ohmic contact is on the right, the drain one on the left.

## III. SINGLE DEVICES ELECTRICAL CHARACTERISTICS AND MODELING

Several power devices were designed on this wafer, from 2x50 $\mu$ m test cells to 8x75 $\mu$ m power transistors. Given the measured small-signal Maximum Gain characteristics, the larger devices available for amplifiers designs at 20GHz and 26.5GHz are respectively 8x75 $\mu$ m and 4x75 $\mu$ m devices (0.6 and 0.3mm total gate lengths). Fig. 2 shows the MSG (Maximum Stable Gain) and MAG (Maximum Available Gain) values measured at V<sub>ds</sub>=15V and I<sub>ds</sub>=100mA. The 8x7 $\mu$ m devices show a MSG of 10.1dB at 20GHz ; the 4x75 $\mu$ m devices show a MAG of 9dB at 26.5GHz. The MSG/MAG transitions are respectively at 22.5 and 26GHz.

Fig. 3 presents the measured load-Pull characteristics for a  $8 \times 75 \mu\text{m}$  at 10GHz in cw RF operation at  $I_{ds}=300\text{mA/mm}$ ,  $V_{ds} = 20\text{V}$ . Table 1 gives the main power characteristics measured for  $V_{ds}$  from 15V to 30V. Unfortunately, no power measurements have been done at 20GHz. Then, the non-linear model [7] has been verified on these measurements at 10GHz. Simulations with this model at 20GHz give an optimum output power of 4.5W/mm with an associated PAE of 31% and a power gain of 5.7dB at 4.2dB compression, at  $V_{ds}=20\text{V}$  and  $I_{ds}=270\text{mA/mm}$ . The model of the  $4 \times 75 \mu\text{m}$  transistor is scaled from the  $8 \times 75 \mu\text{m}$  one.

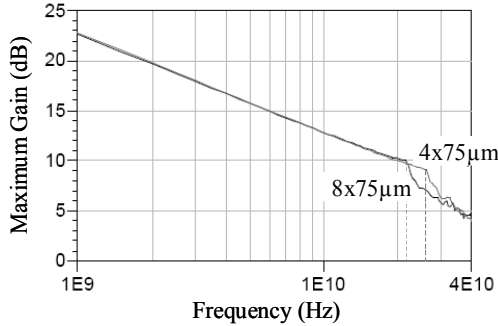


Fig. 2. Maximum gains of  $8 \times 75 \mu\text{m}$  and  $4 \times 75 \mu\text{m}$  transistors at  $V_{ds}=15\text{V}$ ,  $I_{ds}=100\text{mA/mm}$ . The MSG/MAG transitions of the  $8 \times 75 \mu\text{m}$  and  $4 \times 75 \mu\text{m}$  devices are respectively at 22.5GHz and 26GHz. The MSG of the  $8 \times 75 \mu\text{m}$  device is 10.1dB at 20GHz, the MAG of the  $4 \times 75 \mu\text{m}$  device is 9dB at 26.5GHz.

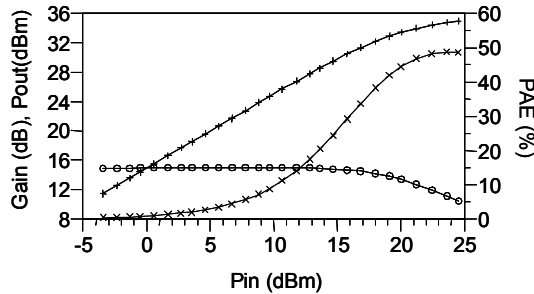


Fig. 3. Cw RF power characteristics of a  $8 \times 75 \mu\text{m}$  transistor at 10GHz in class AB for  $I_{ds}=300\text{mA/mm}$ ,  $V_{ds}=20\text{V}$ .

TABLE I  
MEASURED POWER CHARACTERISTICS OF A  $8 \times 75 \mu\text{m}$  VERSUS DRAIN BIAS VOLTAGE AT 10GHz

	$V_{ds}=15\text{V}$	$V_{ds}=20\text{V}$	$V_{ds}=25\text{V}$	$V_{ds}=30\text{V}$
Pout (W/mm)	3.5	4.7	6.3	7
PAE (%)	51	49	44	39
Gain (linear gain) (dB)	11 (15.4)	11.6 (15.7)	10.35 (15.5)	10.2 (14.8)

## II. HYBRID AMPLIFIERS DESIGN AND FABRICATION

Two amplifiers have been designed for cw RF operation at 20 and 26.5GHz. Hybrid versions have been preferred to MMIC approach for circuit post-tuning capabilities. For the 20GHz

version, 5W were targetted ; for the 26.5GHz version, 2W. In order to improve the thermal management and reduce the parasitics, the transistors are reported in flip-chip over  $254 \mu\text{m}$  AlN substrates. The substrate process allows the realization of on-chip thin-film resistances, but MIM capacitors have to be added on the substrate. Both amplifiers have two stages with 2 transistors each. For the 20GHz amplifier, only  $8 \times 75 \mu\text{m}$  transistors were used for both stages. For the 26.5GHz version, only  $4 \times 75 \mu\text{m}$  devices. Classical single ended amplifier designs are used, which are not the subject of this paper. Fig. 5 shows a photograph of the amplifier mounted in its test jig.

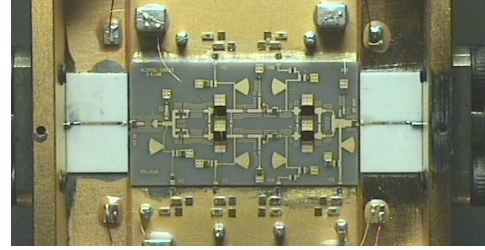


Fig. 5. Photograph of the 20GHz amplifier in its test jig. The AlN chip size is approximately  $18 \times 10 \text{mm}$ .

## II. HYBRID AMPLIFIERS CHARACTERIZATIONS

Power measurements have been performed on both amplifiers. After on chip matching tuning on the 20GHz version, the low level gain has been improved of 1.2dB. It delivers 4.5W with 20% of PAE, a power gain of 7.5dB (12.5dB of linear gain) and  $-11\text{dB}$  return losses in the AlN chip reference planes for a bias point at  $V_{ds_{1st\_stage}}=18\text{V}$ ,  $V_{ds_{2nd\_stage}}=20\text{V}$ ,  $I_{ds}=250\text{mA/mm}$ , at 20GHz. Fig. 6 shows the measured and simulated power characteristics at 20GHz. Considering the fairly good correlation between measurements and simulations, this allows to estimate the power stage devices power characteristics: they deliver an output power of 4.1W/mm with 28% PAE, which is very close to the maximum power density foreseen by the transistor model (the simulated losses of the output matching circuit are 0.36dB at 20GHz). Measurements have also been done at higher bias voltages for each stage up to  $V_{ds}=25\text{V}$  but contrarily to simulation results, the power characteristics do not increase. Consequently, an estimation of the device temperature has been done thanks to 3D-FEM simulations that show that the junction temperature of the 2<sup>nd</sup> stage transistors reaches  $230^\circ\text{C}$  in the nominal case ( $V_{ds_{2nd\_stage}}=20\text{V}$ ). The thermal management would be improved in a future MMIC version, taking advantage of the 2.3 times better thermal conductivity of the SiC substrate if compared to the AlN. This could also allow to improve the parasitic source inductance, which is evaluated to 30pH in addition to the transistor own source inductance. It induces a gain loss of  $\sim 2.5\text{dB}$  per stage at 20GHz.

The second amplifier delivers at 26.5GHz a cw output power of 1.3W with 13% PAE, a power gain of 8.3dB (13.2dB of linear gain) and  $-8$ dB return losses in the AIN chip reference planes for a bias point at  $V_{ds1st\ stage}=18V$ ,  $V_{ds2nd\ stage}=20V$ ,  $I_{ds}=270mA/mm$ . A frequency sweep shows a bandwidth of approximately 1GHz (4%) around 26GHz, as Fig. 8 illustrates it. A second amplifier delivered, at 26.5GHz, a cw output power of 1.65W with 15.5% PAE with an associated power gain of 7.6dB, i.e. at higher compression. Despite the lower PAE than for the 20GHz amplifier, the power dissipation is lower here as it reaches 7.3W/mm at compression, whereas it reaches 9.5W/mm in the 20GHz version. The estimated 2<sup>nd</sup> stage transistors junction temperature is 160°C in this case.

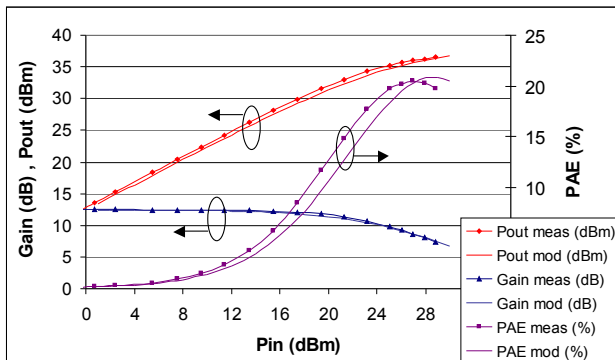


Fig. 6. Measured and simulated power characteristics at the nominal bias point of the 20GHz amplifier.

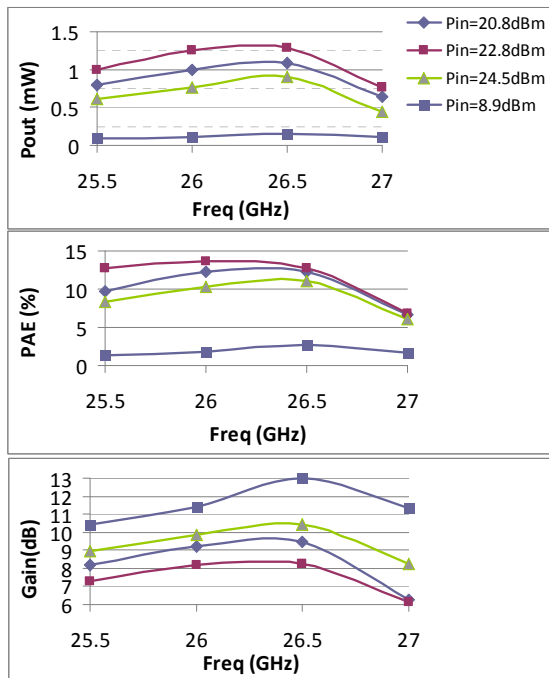


Fig. 8. Power performances of a 26.5GHz amplifier between 25.5GHz and 26.5GHz. for input powers from 8.9dBm to 24.5dBm.

## VII. CONCLUSION

Two K-band amplifiers have been designed, using AlInN/GaN devices. The first version delivers 4.5W with 20% of PAE at 20GHz, and the second version 1.65W with 15.5% of PAE at 26.5GHz. These very good performances obtained with 0.25 $\mu$ m gate length devices that could be improved using shorter gates in a future work show the interest for this technology at high frequencies, and also the potential of AlInN/GaN HEMTs to operate at high temperature.

## ACKNOWLEDGEMENT

The authors would like to acknowledge the French Space Agency "Centre National des Etudes Spatiales (CNES)" for financial support under the contract "93160/00", and the French "Direction Générale de l'Armement (DGA-MI)" for process evaluation support.

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